19-3035; Rev 1; 11/03

MAXIM

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

General Description

The MAX5065/MAX5067 dual-phase, PWM controllers provide high-output-current capability in a compact package with a minimum number of external components. The MAX5065/MAX5067 utilize a dual-phase, average-current-mode control that enables optimal use of low $R_{DS(ON)}$ MOSFETs, eliminating the need for external heatsinks even when delivering high output currents.

Differential sensing enables accurate control of the output voltage, while adaptive voltage positioning provides optimum transient response. An internal regulator enables operation with input voltage ranges of +4.75V to +5.5V or +8V to +28V. The high switching frequency, up to 500kHz per phase, and dual-phase operation allow the use of low-output inductor values and input capacitor values. This accommodates the use of PC board-embedded planar magnetics achieving superior reliability, current sharing, thermal management, compact size, and low system cost.

The MAX5065/MAX5067 also feature a clock input (CLKIN) for synchronization to an external clock, and a clock output (CLKOUT) with programmable phase delay (relative to CLKIN) for paralleling multiple phases. The MAX5065/MAX5067 also limit the reverse current if the bus voltage becomes higher than the regulated output voltage. These devices are specifically designed to limit current sinking when multiple power-supply modules are paralleled. The MAX5065 offers an adjustable +0.6V to +3.3V output voltage. The MAX5067 output voltage is adjustable from +0.8V to +3.3V and features an overvoltage protection and a power-good output signal.

The MAX5065/MAX5067 operate over the extended temperature range (-40°C to +85°C). The MAX5065 is available in a 28-pin SSOP package. The MAX5067 is available in a 44-pin thin QFN package. Refer to the MAX5037A data sheet for a VRM 9.0/VRM 9.1-compatible, VID-controlled output voltage controller in a 44-pin QFN package.

Applications

Servers and Workstations

Point-of-Load High-Current/High-Density Telecom DC-DC Regulators

Networking Systems

Large-Memory Arrays

RAID Systems

High-End Desktop Computers

Features

- **+4.75V to +5.5V or +8V to +28V Input Voltage Range**
- **Adjustable V_{OUT}**
  - **+0.6V to +3.3V (MAX5065)**
  - **+0.8V to +3.3V (MAX5067)**
- **Up to 60A Output Current**
- **Internal Voltage Regulator for a +12V or +24V Power Bus**
- **Programmable Adaptive Output Voltage Positioning**
- **True Differential Remote Output Sensing**
- **Out-of-Phase Controllers Reduce Input Capacitance Requirement and Distribute Power Dissipation**
- **Average-Current-Mode Control**
  - **Superior Current Sharing Between Individual Phases and Paralleled Modules**
  - **Accurate Current Limit Eliminates MOSFET and Inductor Derating**
- **Limits Reverse-Current Sinking in Paralleled Modules**
- **Integrated 4A Gate Drivers**
- **Selectable Fixed Frequency 250kHz or 500kHz Per Phase (Up to 1MHz for Two Phases)**
- **External Frequency Synchronization from 125kHz to 600kHz**
- **Internal PLL with Clock Output for Paralleling Multiple DC-DC Converters**
- **Thermal Protection**
- **28-Pin SSOP Package (MAX5065)**
- **44-Pin Thin QFN Package (MAX5067)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5065EAI	-40°C to +85°C	28 SSOP
MAX5067ETH	-40°C to +85°C	44 Thin QFN

Selector Guide and Pin Configurations appear at end of data sheet.

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

ABSOLUTE MAXIMUM RATINGS

IN to SGND .....-0.3V to +30V
BST_ to SGND .....-0.3V to +35V
DH_ to LX_ .....-0.3V to [($V_{BST\_}$ - $V_{LX\_}$) + 0.3V]
DL_ to PGND .....-0.3V to (V_{CC} + 0.3V)
BST_ to LX_ .....-0.3V to +6V
V_{CC} to SGND .....-0.3V to +6V
V_{CC}, V_{DD} to PGND .....-0.3V to +6V
SGND to PGND .....-0.3V to +0.3V
All Other Pins to SGND.....-0.3V to (V_{CC} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derate 9.5mW/°C above +70°C) 762mW
44-Pin Thin QFN (derate 27.0mW/°C above+70°C) ...2162mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS							
Input Voltage Range	V_{IN}			8		28	V
		Short IN and V_{CC} together for +5V input operation		4.75		5.50	
Quiescent Supply Current	I_Q	EN = V_{CC} or SGND			4	10	mA
Efficiency	η	I_{LOAD} = 52A (26A per phase)			90		%
OUTPUT VOLTAGE							
SENSE+ to SENSE- Accuracy (Note 4)		MAX5065	No load	0.5952	0.6	0.6048	V
			No load, V_{CC} = +4.75V to +5.5V or V_{IN} = +8V to +28V	0.594	0.6	0.6064	
		MAX5067	No load	0.7936	0.8	0.8064	
			No load, V_{CC} = +4.75V to +5.5V or V_{IN} = +8V to +28V	0.792	0.8	0.808	
STARTUP/INTERNAL REGULATOR							
V_{CC} Undervoltage Lockout	UVLO	V_{CC} rising		4.0	4.15	4.5	V
V_{CC} Undervoltage Lockout Hysteresis					200		mV
V_{CC} Output Accuracy		V_{IN} = +8V to +28V, I_{SOURCE} = 0 to 80mA		4.85	5.1	5.30	V
MOSFET DRIVERS							
Output Driver Impedance	R_{ON}	Low or high output			1	3	Ω
Output Driver Source/Sink Current	$I_{DH\_}$, $I_{DL\_}$				4		A
Nonoverlap Time	t_{NO}	$C_{DH\_/DL\_}$ = 5nF			60		ns
OSCILLATOR AND PLL							
Switching Frequency	f_{SW}	CLKIN = SGND		238	250	262	kHz
		CLKIN = V_{CC}		475	500	525	
PLL Lock Range	f_{PLL}			125		600	kHz
PLL Locking Time	t_{PLL}				200		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLKOUT Phase Shift (At f_{SW} = 125kHz)	ϕ_{CLKOUT}	PHASE = V_{CC}	115	120	125	degrees
		PHASE = unconnected	85	90	95	
		PHASE = SGND	55	60	65	
CLKIN Input Pulldown Current	I_{CLKIN}		3	5	7	µA
CLKIN High Threshold	V_{CLKINH}		2.4			V
CLKIN Low Threshold	V_{CLKINL}				0.8	V
CLKIN High Pulse Width	t_{CLKIN}		200			ns
PHASE High Threshold	V_{PHASEH}		4			V
PHASE Low Threshold	V_{PHASEL}				1	V
PHASE Input Bias Current	$I_{PHASEBIAS}$		-50		+50	µA
CLKOUT Output Low Level	$V_{CLKOUTL}$	I_{SINK} = 2mA (Note 2)			100	mV
CLKOUT Output High Level	$V_{CLKOUTH}$	I_{SOURCE} = 2mA (Note 2)	4.5			V
CURRENT LIMIT						
Average Current-Limit Threshold	V_{CL}	CSP_ to CSN_	45	48	51	mV
Reverse Current-Limit Threshold	V_{CLR}	CSP_ to CSN_	-3.9		-0.2	mV
Cycle-by-Cycle Current Limit	V_{CLPK}	CSP_ to CSN_ (Note 3)	90	112	130	mV
Cycle-by-Cycle Overload Response Time	t_R	$V_{CSP\_}$ to $V_{CSN\_}$ = +150mV		260		ns
CURRENT-SENSE AMPLIFIER						
CSP_ to CSN_ Input Resistance	$R_{CS\_}$			4		kΩ
Common-Mode Range	$V_{CMR(CS)}$		-0.3		+3.6	V
Input Offset Voltage	$V_{OS(CS)}$		-1		+1	mV
Amplifier Gain	$A_{V(CS)}$			18		V/V
3dB Bandwidth	f_{3dB}			4		MHz
CURRENT-ERROR AMPLIFIER (TRANSCONDUCTANCE AMPLIFIER)						
Transconductance	gm_{ca}			550		µS
Open-Loop Gain	$A_{VOL(CE)}$	No load		50		dB
DIFFERENTIAL VOLTAGE AMPLIFIER (DIFF)						
Common-Mode Voltage Range	$V_{CMR(DIFF)}$		-0.3		+1.0	V
DIFF Output Voltage	V_{CM}	V_{SENSE+} = V_{SENSE-} = 0		0.6		V
Input Offset Voltage	$V_{OS(DIFF)}$		-1		+1	mV
Amplifier Gain	$A_{V(DIFF)}$		0.997	1	1.003	V/V
3dB Bandwidth	f_{3dB}	C_{DIFF} = 20pF		3		MHz
Minimum Output Current Drive	$I_{OUT(DIFF)}$		1.0			mA
SENSE+ to SENSE- Input Resistance	$R_{VS\_}$		50	100		kΩ

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE-ERROR AMPLIFIER (EAOUT)						
Open-Loop Gain	$A_{VOL(EA)}$			70		dB
Unity-Gain Bandwidth	f_{UGEA}			3		MHz
EAN Input Bias Current	$I_{B(EA)}$	V_{EAN} = +2.0V	-100		+100	nA
Error-Amplifier Output Clamping Voltage	$V_{CLAMP(EA)}$	With respect to V_{CM}	810		918	mV
POWER-GOOD, PHASE FAILURE DETECTION, OVERVOLTAGE PROTECTION, AND THERMAL SHUTDOWN						
PGOOD Trip Level (MAX5067)	V_{OV}	PGOOD goes low when V_{OUT} is outside this window	+6	+8	+10	$\%V_{OUT}$
	V_{UV}	PGOOD goes low when V_{OUT} is outside this window	-12.5	-10	-8.5	
PGOOD Output Low Level (MAX5067)	V_{PGLO}	I_{SINK} = 4mA			0.2	V
PGOOD Output Leakage Current (MAX5067)	I_{PG}	PGOOD = V_{CC}			1	µA
Phase Failure Trip Threshold (MAX5067)	V_{PH}	PGOOD goes low when CLP_ is higher than V_{PH}		2		V
OVPIN Trip Threshold (MAX5067)	OVP_{TH}	With respect to SGND	0.792	0.8	0.808	V
OVPIN Input Resistance (MAX5067)	R_{OVPIN}		190	280	370	kΩ
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SHDN}			150		°C
Thermal-Shutdown Hysteresis				8		°C
EN INPUT						
EN Input Low Voltage	V_{ENL}				1	V
EN Input High Voltage	V_{ENH}		3			V
EN Pullup Current	I_{EN}		4.5	5	5.5	µA

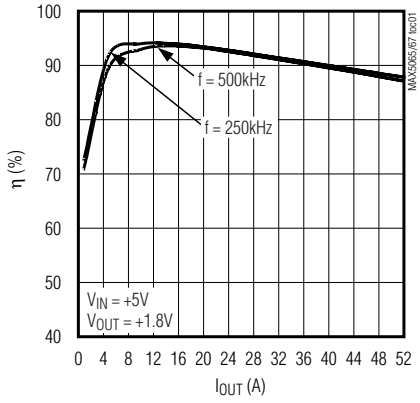
Note 1: Specifications from -40°C to 0°C are guaranteed by characterization but not production tested.
Note 2: Guaranteed by design. Not production tested.
Note 3: See *Peak-Current Comparator* section.
Note 4: Does not include an error due to finite error amplifier gain. See the *Voltage-Error Amplifier* section.

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

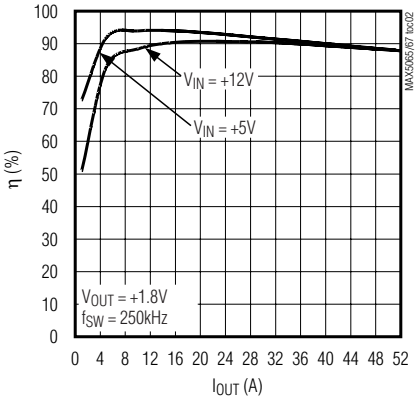
Typical Operating Characteristics

(Circuit of Figure 1. T_A = +25°C, unless otherwise noted.)

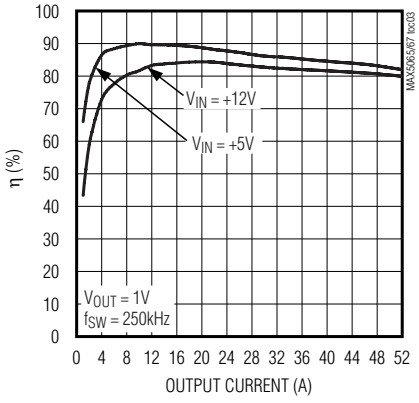
EFFICIENCY vs. OUTPUT CURRENT AND INTERNAL OSCILLATOR FREQUENCY



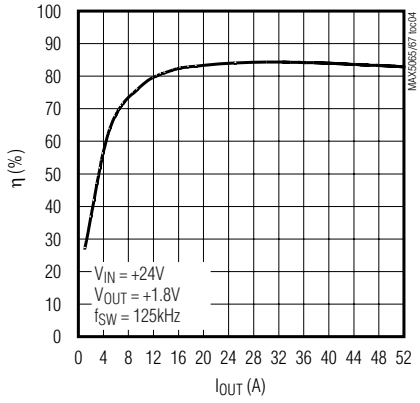
EFFICIENCY vs. OUTPUT CURRENT AND INPUT VOLTAGE



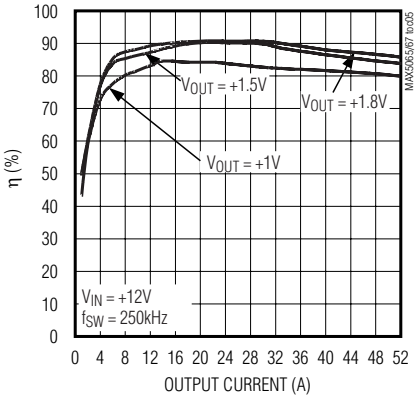
EFFICIENCY vs. OUTPUT CURRENT AND INPUT VOLTAGE



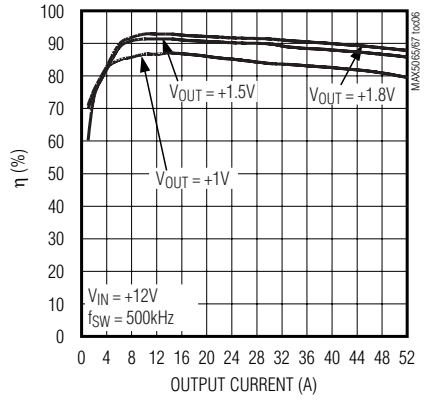
EFFICIENCY vs. OUTPUT CURRENT



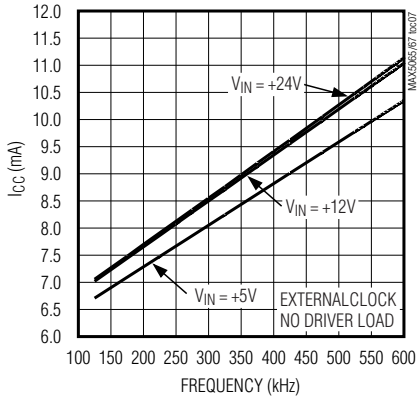
EFFICIENCY vs. OUTPUT CURRENT AND OUTPUT VOLTAGE



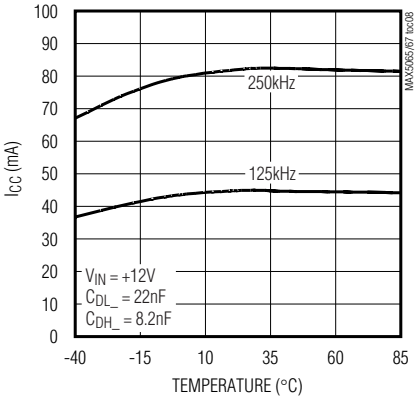
EFFICIENCY vs. OUTPUT CURRENT AND OUTPUT VOLTAGE



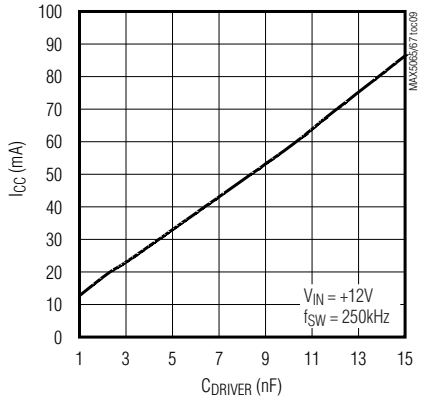
SUPPLY CURRENT vs. FREQUENCY AND INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE AND FREQUENCY



SUPPLY CURRENT vs. LOAD CAPACITANCE PER DRIVER

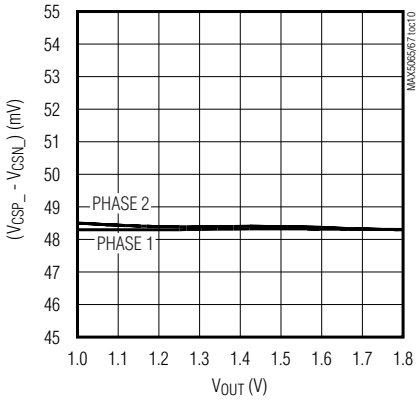


Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

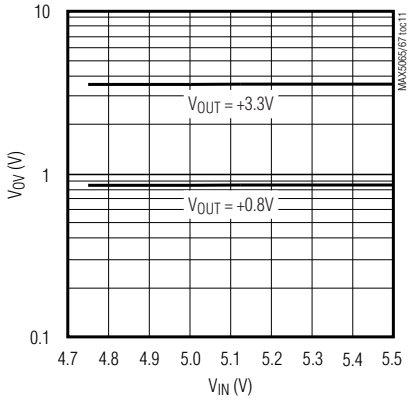
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

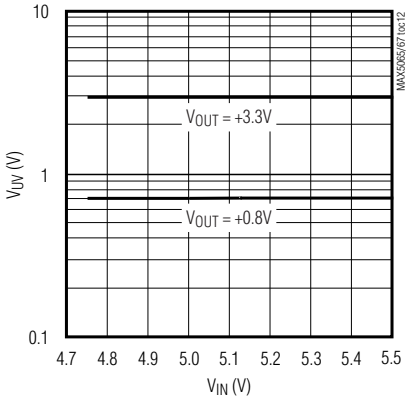
CURRENT-SENSE THRESHOLD vs. OUTPUT VOLTAGE



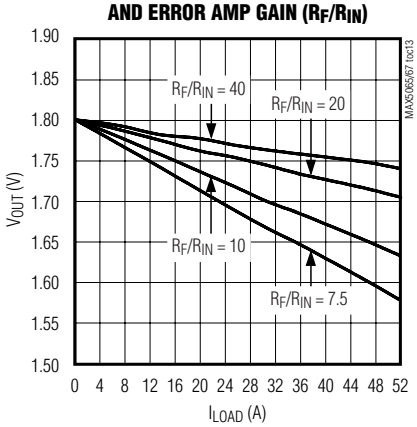
OVERVOLTAGE THRESHOLD (PGOOD) vs. INPUT VOLTAGE



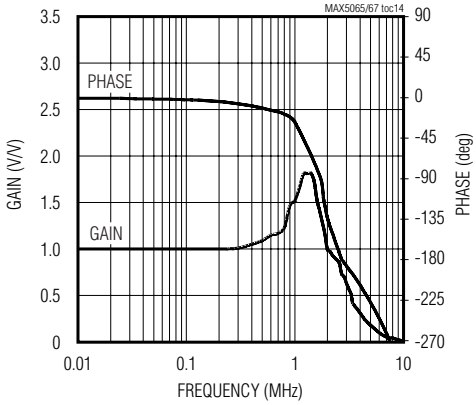
UNDERVOLTAGE THRESHOLD (PGOOD) vs. INPUT VOLTAGE



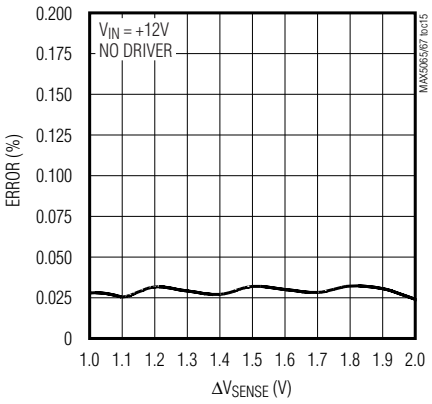
OUTPUT VOLTAGE vs. OUTPUT CURRENT AND ERROR AMP GAIN (R_F/R_{IN})



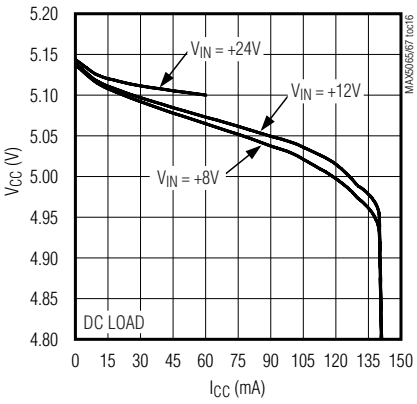
DIFFERENTIAL AMPLIFIER BANDWIDTH



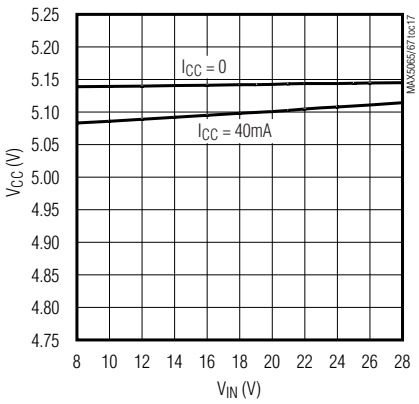
DIFF OUTPUT ERROR vs. SENSE+ TO SENSE- VOLTAGE



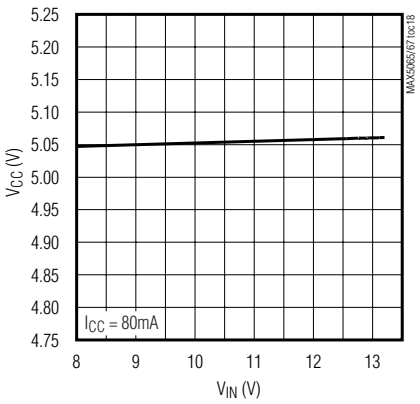
VCC LOAD REGULATION vs. INPUT VOLTAGE



VCC LINE REGULATION



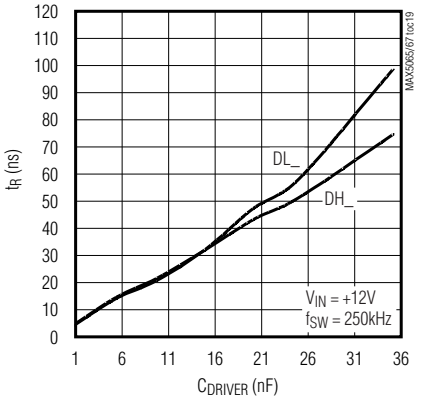
VCC LINE REGULATION



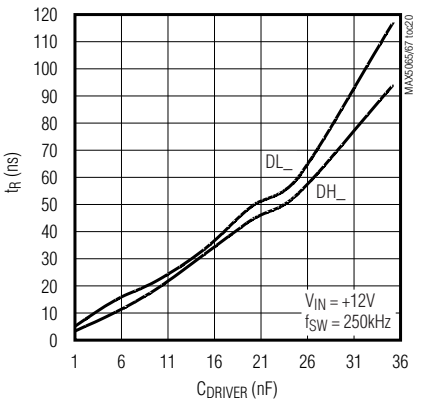
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

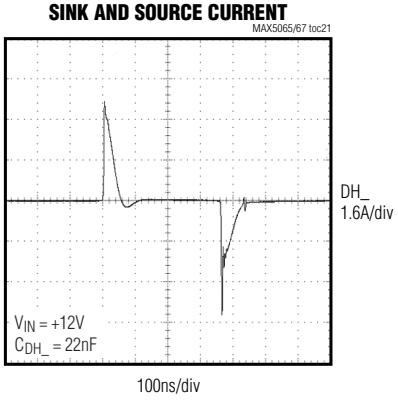
DRIVER RISE TIME vs. DRIVER LOAD CAPACITANCE



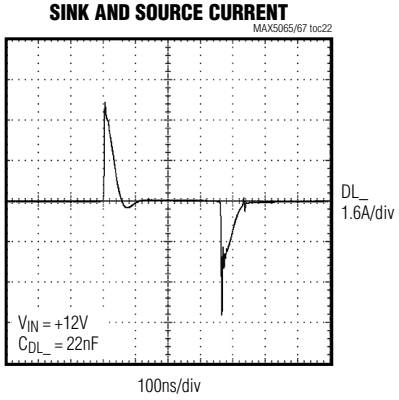
DRIVER FALL TIME vs. DRIVER LOAD CAPACITANCE



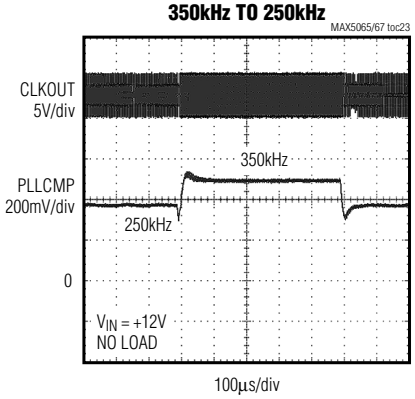
HIGH-SIDE DRIVER (DH_) SINK AND SOURCE CURRENT



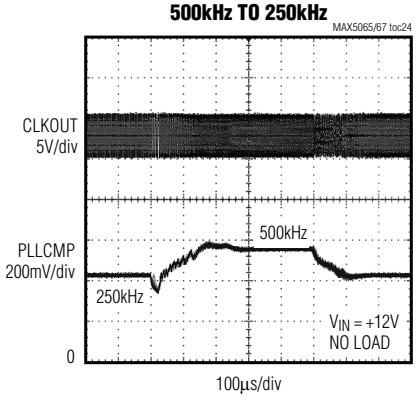
LOW-SIDE DRIVER (DL_) SINK AND SOURCE CURRENT



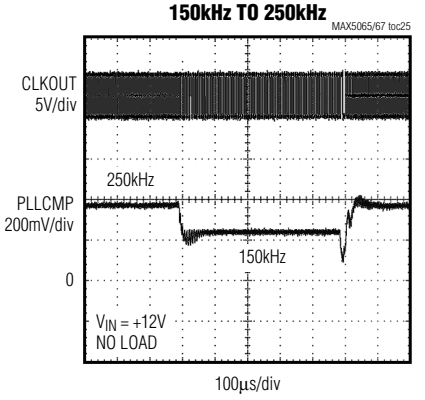
PLL LOCKING TIME 250kHz TO 350kHz AND 350kHz TO 250kHz



PLL LOCKING TIME 250kHz TO 500kHz AND 500kHz TO 250kHz



PLL LOCKING TIME 250kHz TO 150kHz AND 150kHz TO 250kHz

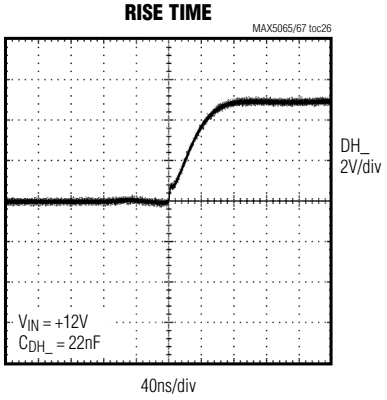


Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

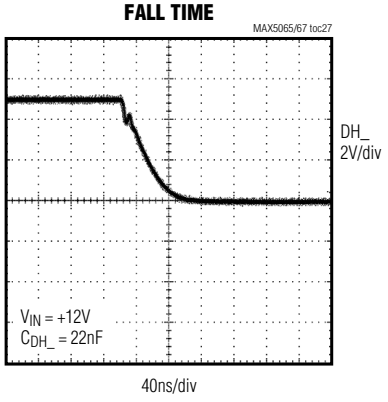
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

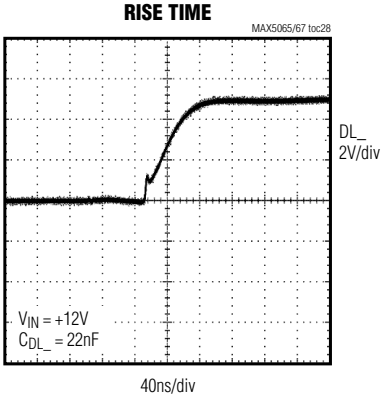
HIGH-SIDE DRIVER (DH_) RISE TIME



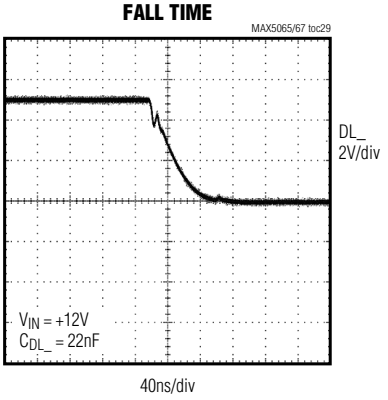
HIGH-SIDE DRIVER (DH_) FALL TIME



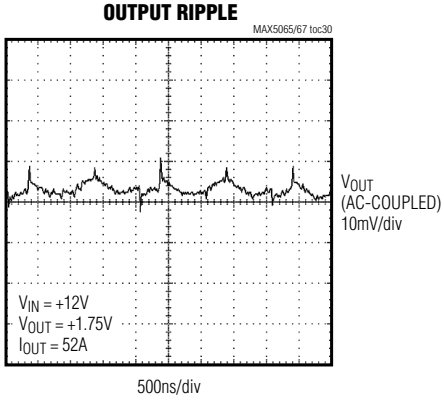
LOW-SIDE DRIVER (DL_) RISE TIME



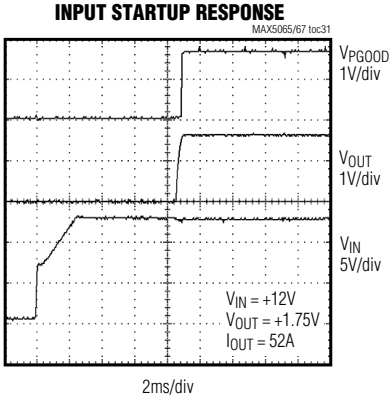
LOW-SIDE DRIVER (DL_) FALL TIME



OUTPUT RIPPLE



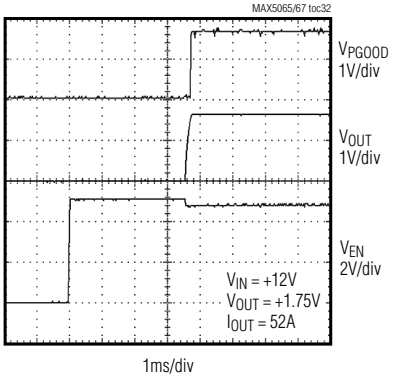
INPUT STARTUP RESPONSE



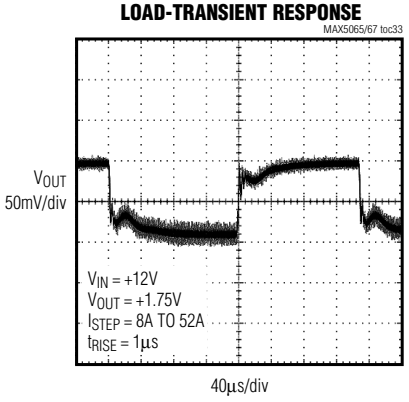
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

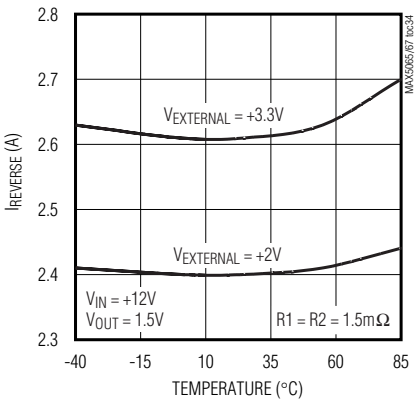
ENABLE STARTUP RESPONSE



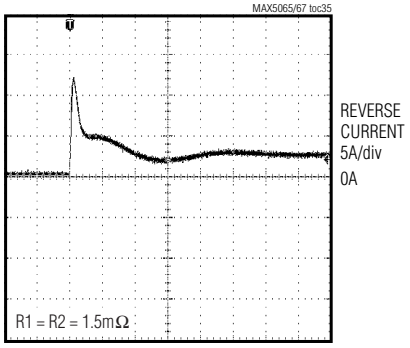
LOAD-TRANSIENT RESPONSE



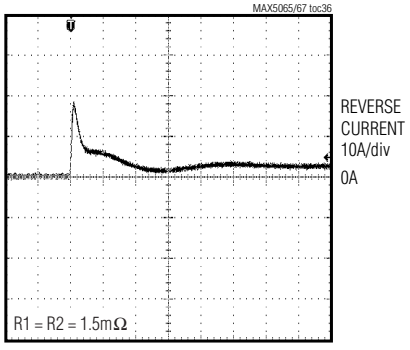
REVERSE CURRENT SINK vs. TEMPERATURE



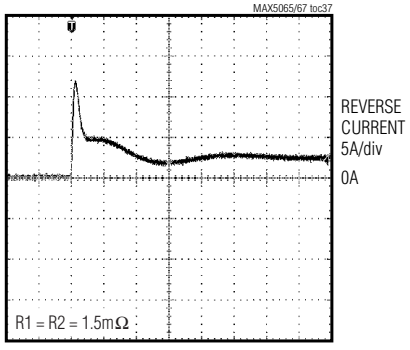
REVERSE CURRENT SINK AT INPUT TURN-ON (V_{IN} = 12V, V_{OUT} = 1.5V, $V_{EXTERNAL}$ = 2.5V)



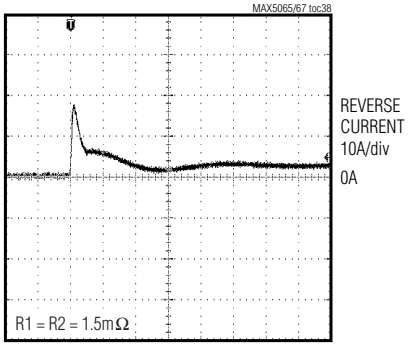
REVERSE CURRENT SINK AT INPUT TURN-ON (V_{IN} = 12V, V_{OUT} = 1.5V, $V_{EXTERNAL}$ = 3.3V)



REVERSE CURRENT SINK AT ENABLE TURN-ON (V_{IN} = 12V, V_{OUT} = 1.5V, $V_{EXTERNAL}$ = 2.5V)



REVERSE CURRENT SINK AT ENABLE TURN-ON (V_{IN} = 12V, V_{OUT} = 1.5V, $V_{EXTERNAL}$ = 3.3V)



Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

Pin Description

PIN		NAME	FUNCTION
MAX5065	MAX5067		
1, 13	39, 16	CSP2, CSP1	Current-Sense Differential Amplifier Positive Inputs. Sense the inductor current. The differential voltage between CSP_ and CSN_ is amplified internally by the current-sense amplifier gain of 18.
2, 14	40, 17	CSN2, CSN1	Current-Sense Differential Amplifier Negative Inputs. Together with CSP_, sense the inductor current.
3	41	PHASE	Phase-Shift Setting Input. Connect PHASE to V_{CC} for 120°, leave PHASE unconnected for 90°, or connect PHASE to SGND for 60° of phase shift between the rising edge of CLKOUT and CLKIN/DH1.
4	42	PLLCMP	External Loop-Compensation Input. Connect compensation network for the phase-locked loop (see the *Phase-Locked Loop* section).
5, 7	43, 7	CLP2, CLP1	Current-Error Amplifier Outputs. Compensate the current loop by connecting an RC network to ground.
6	5, 20, 35	SGND	Signal Ground. Ground connection for the internal control circuitry.
8	10	SENSE+	Differential Output-Voltage-Sensing Positive Input. Used to sense a remote load. The MAX5065 and MAX5067 regulate the difference between SENSE+ and SENSE- according to the factory preset reference voltage of +0.6V and +0.8V, respectively.
9	11	SENSE-	Differential Output Voltage-Sensing Negative Input. Used to sense a remote load. Connect SENSE- to V_{OUT-} or PGND at the load.
10	12	DIFF	Differential Remote-Sense Amplifier Output. DIFF is the output of a precision unity-gain amplifier.
11	13	EAN	Voltage-Error Amplifier Inverting Input. Receives a signal from the output of the differential remote-sense amplifier. Referenced to SGND.
12	14	EAOUT	Voltage-Error Amplifier Output. Connect to the external gain-setting feedback resistor. The external error amplifier gain-setting resistors determine the amount of adaptive voltage positioning.
15	19	EN	Output Enable. A logic-low shuts down the power drivers. EN has an internal 5µA pullup current.
16, 26	22, 34	BST1, BST2	Boost Flying-Capacitor Connection. Reservoir capacitor connection for the high-side FET driver supply. Connect a 0.47µF ceramic capacitor between BST_ and LX_.
17, 25	23, 32	DH1, DH2	High-Side Gate-Driver Outputs. Drive the gate of the high-side MOSFET.
18, 24	24, 31	LX1, LX2	Inductor Connection. Source connection for the high-side MOSFETs. Also serve as the return terminal for the high-side driver.
19, 23	25, 30	DL1, DL2	Low-Side Gate-Driver Outputs. Synchronous MOSFET gate drivers for the two phases.
20	27	V_{CC}	Internal +5V Regulator Output. V_{CC} is derived internally from the IN voltage. Bypass to SGND with 4.7µF and 0.1µF ceramic capacitors in parallel.
21	28	IN	Supply Voltage Connection. Connect IN to V_{CC} for a +5V system. Connect the unregulated power source to IN through an RC lowpass filter comprised of a 2.2Ω resistor and a 0.1µF ceramic capacitor.
22	29	PGND	Power Ground. Connect the V_{CC} bypass capacitors, input capacitors, output capacitors, and low-side synchronous MOSFET source to PGND.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX5065	MAX5067		
27	36	CLKOUT	Oscillator Output. CLKOUT is phase-shifted from CLKIN by the amount determined by the PHASE input. Use CLKOUT to parallel additional MAX5065/MAX5067s.
28	38	CLKIN	CMOS Logic Clock Input. Drive CLKIN with a frequency range between 125kHz and 600kHz or connect to V_{CC} or SGND. Connect CLKIN to SGND to set the internal oscillator to 250kHz or connect to V_{CC} to set the internal oscillator to 500kHz. CLKIN has an internal 5µA pulldown current.
—	6	OVPIN	Overvoltage Protection Circuit Input. Connect OVPIN to the center of the resistive-divider between V_{OUT} and GND. When OVPIN exceeds +0.8V with respect to SGND, OVPOUT latches DH_ low and DL_ high. Toggle EN low to high or recycle the power to reset the latch.
—	8	OVPOUT	Overvoltage Protection Output. Use the OVPOUT active-high, push-pull output to trigger a safety device such as an SCR.
—	9	PGOOD	Power-Good Output. The open-drain, active-low PGOOD output goes low when the output voltage falls out of regulation or a phase failure is detected. The power-good window-comparator thresholds are +8% and -10% of the output voltage. Forcing EN low also forces PGOOD low.
—	1, 2, 3, 4, 15, 18, 21, 33, 37, 44	N.C.	No Connection. Not internally connected.
—	26	V_{DD}	Supply Voltage for Low-Side and High-Side Drivers. V_{CC} powers V_{DD}. Connect a parallel combination of 0.1µF and 1µF ceramic capacitors to PGND and a 1Ω resistor to V_{CC} to filter out the high peak currents of the driver from the internal circuitry.

Detailed Description

The MAX5065/MAX5067 average-current-mode PWM controllers drive two out-of-phase buck converter channels. Average-current-mode control improves current sharing between the channels while minimizing component derating and size. Parallel multiple MAX5065/MAX5067 regulators to increase the output current capacity. For maximum ripple rejection at the input, set the phase shift between phases to 90° for two paralleled converters, or 60° for three paralleled converters. Paralleling the MAX5065/MAX5067s improves design flexibility in applications requiring upgrades (higher load).

Dual-phase converters with an out-of-phase locking arrangement reduce the input and output capacitor ripple current, effectively multiplying the switching frequency by the number of phases. Each phase of the MAX5065/MAX5067 consists of an inner average current loop controlled by a common outer-loop voltage-error amplifier (VEA). The combined action of the two inner current loops and the outer voltage loop corrects the output voltage errors and forces the phase currents to be equal. Program the output voltage from +0.6V to +3.3V (MAX5065) and +0.8V to +3.3V (MAX5067) using a resistive-divider at SENSE+ and SENSE-.

V_{IN}, V_{CC}, V_{DD}

The MAX5065/MAX5067 accept a wide input voltage range of +4.75V to +5.5V or +8V to +28V. All internal control circuitry operates from an internally regulated nominal voltage of +5V (V_{CC}). For input voltages of +8V or greater, the internal V_{CC} regulator steps the voltage down to +5V. The V_{CC} output voltage regulates to +5V while sourcing up to 80mA. Bypass V_{CC} to SGND with 4.7µF and 0.1µF low-ESR ceramic capacitors for high-frequency noise rejection and stable operation (Figures 1, 2, and 3).

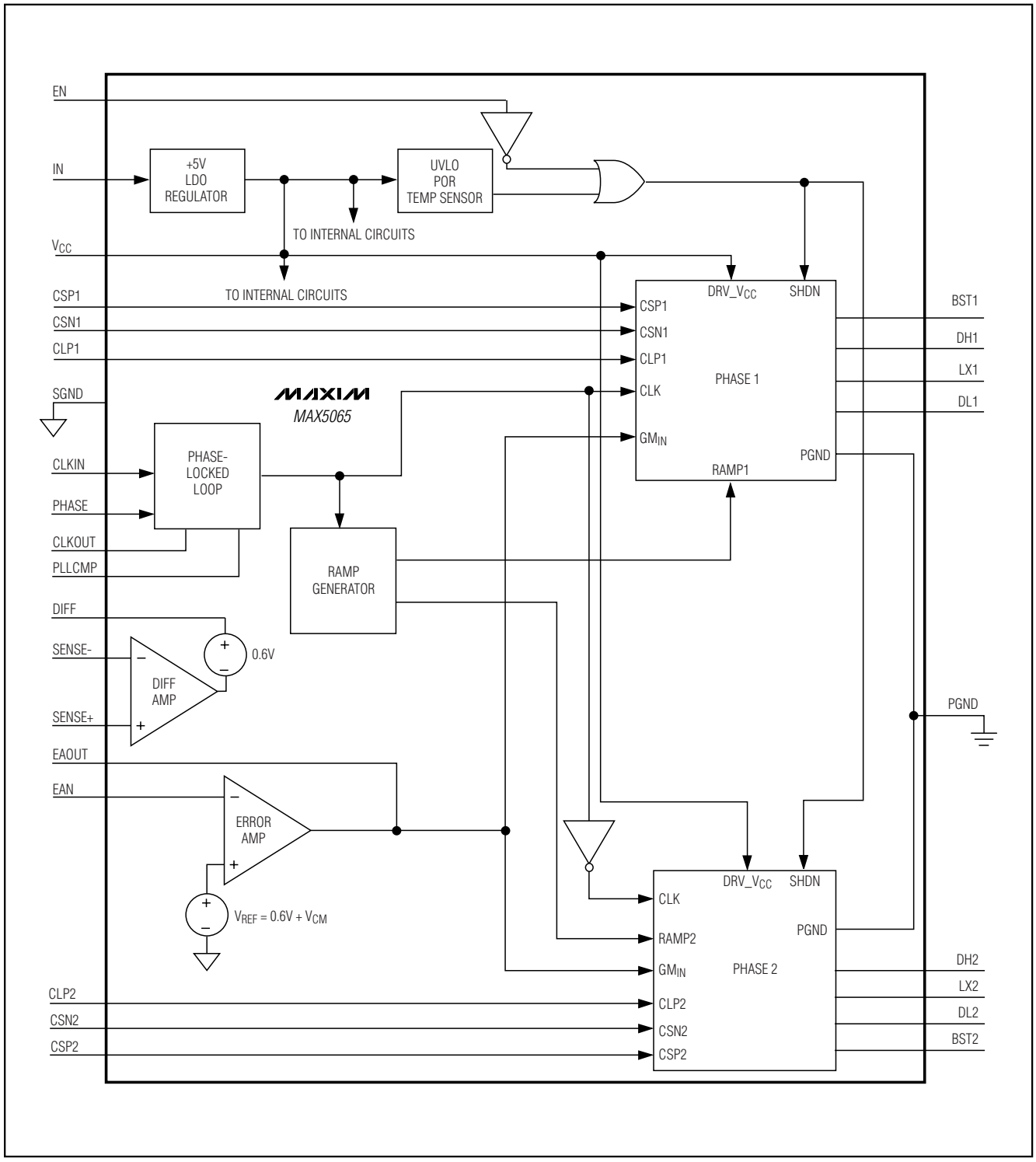
Calculate power dissipation in the MAX5065/MAX5067 as a product of the input voltage and the total V_{CC} regulator output current (I_{CC}). I_{CC} includes quiescent current (I_Q) and gate-drive current (I_{DD}):

$$P_D = V_{IN} \times I_{CC} \quad (1)$$

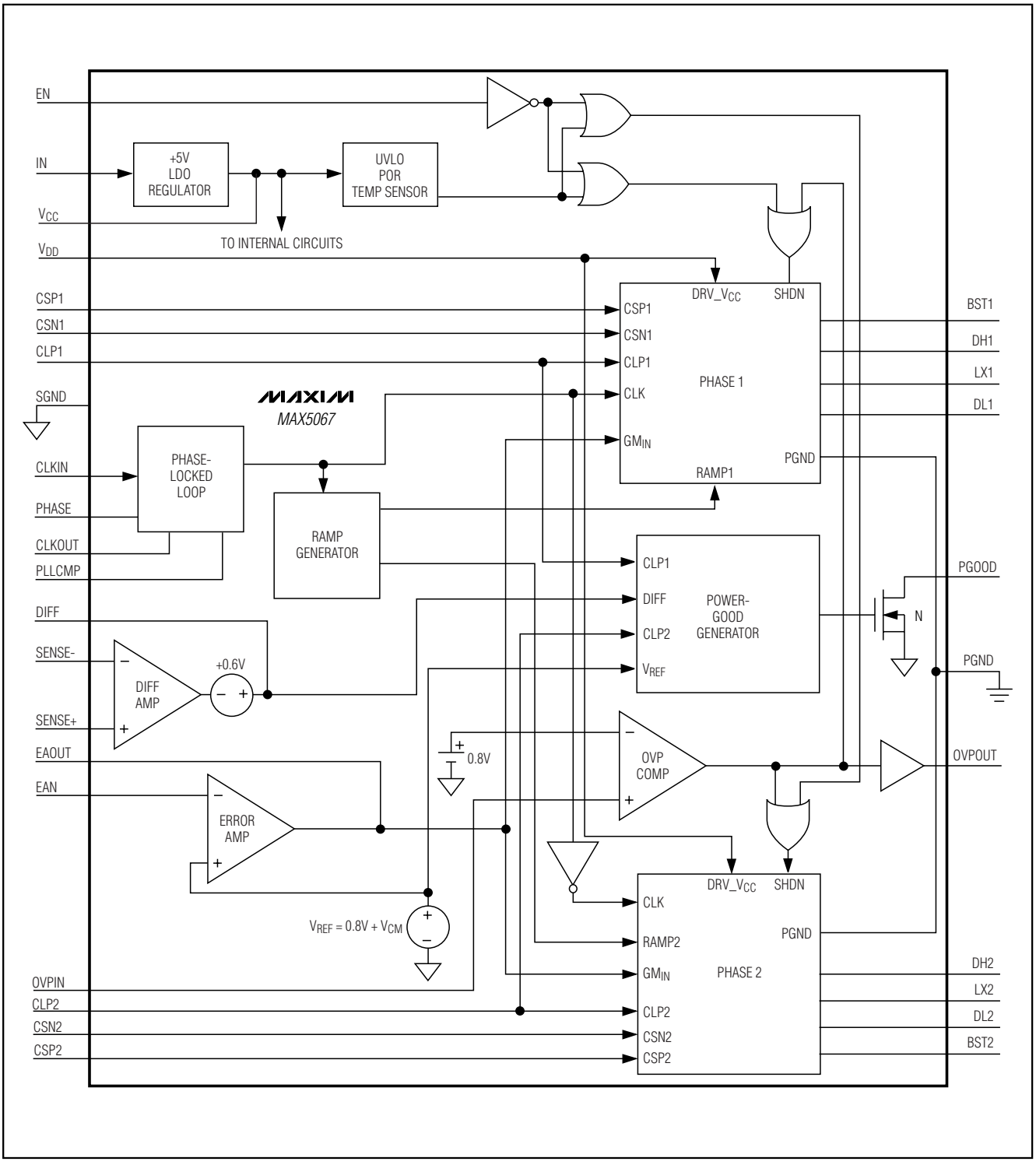
$$I_{CC} = I_Q + f_{SW} \times (Q_{G1} + Q_{G2} + Q_{G3} + Q_{G4}) \quad (2)$$

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

Functional Diagrams



Functional Diagrams (continued)



Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

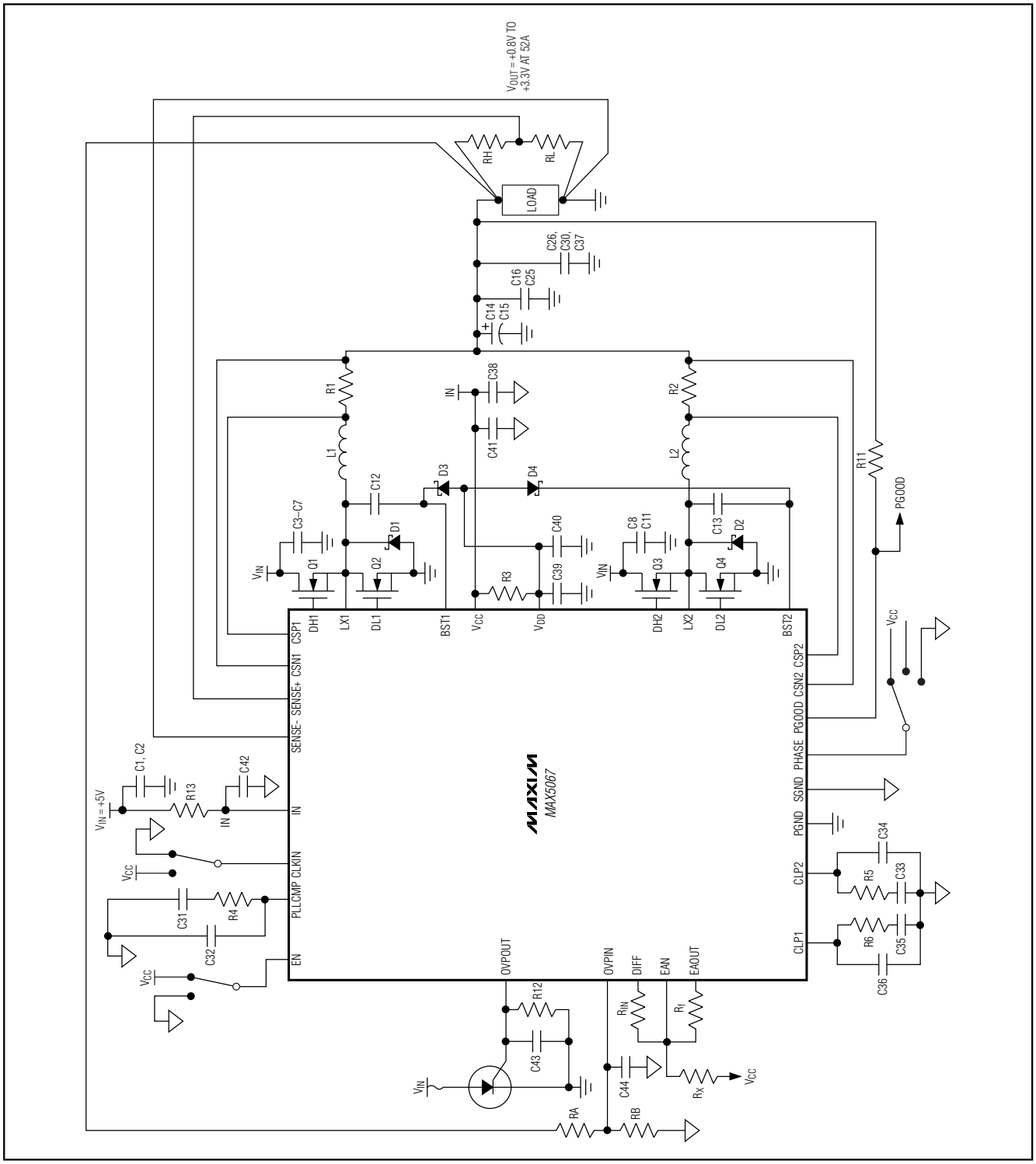


Figure 1. Typical Application Circuit, V_{IN} = +5V

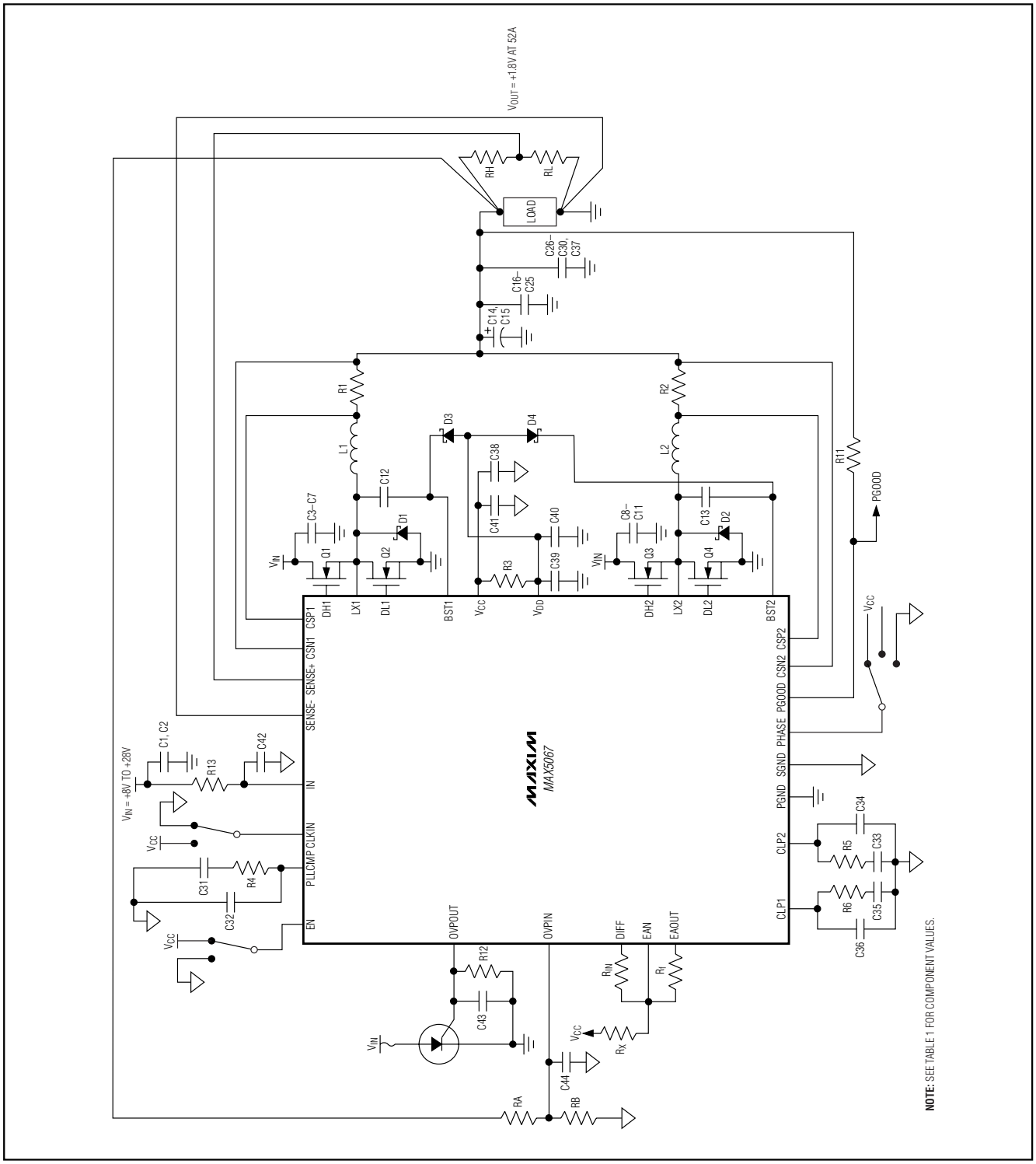


Figure 2. Typical VRM Application Circuit, V_{IN} = +8V to +28V

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

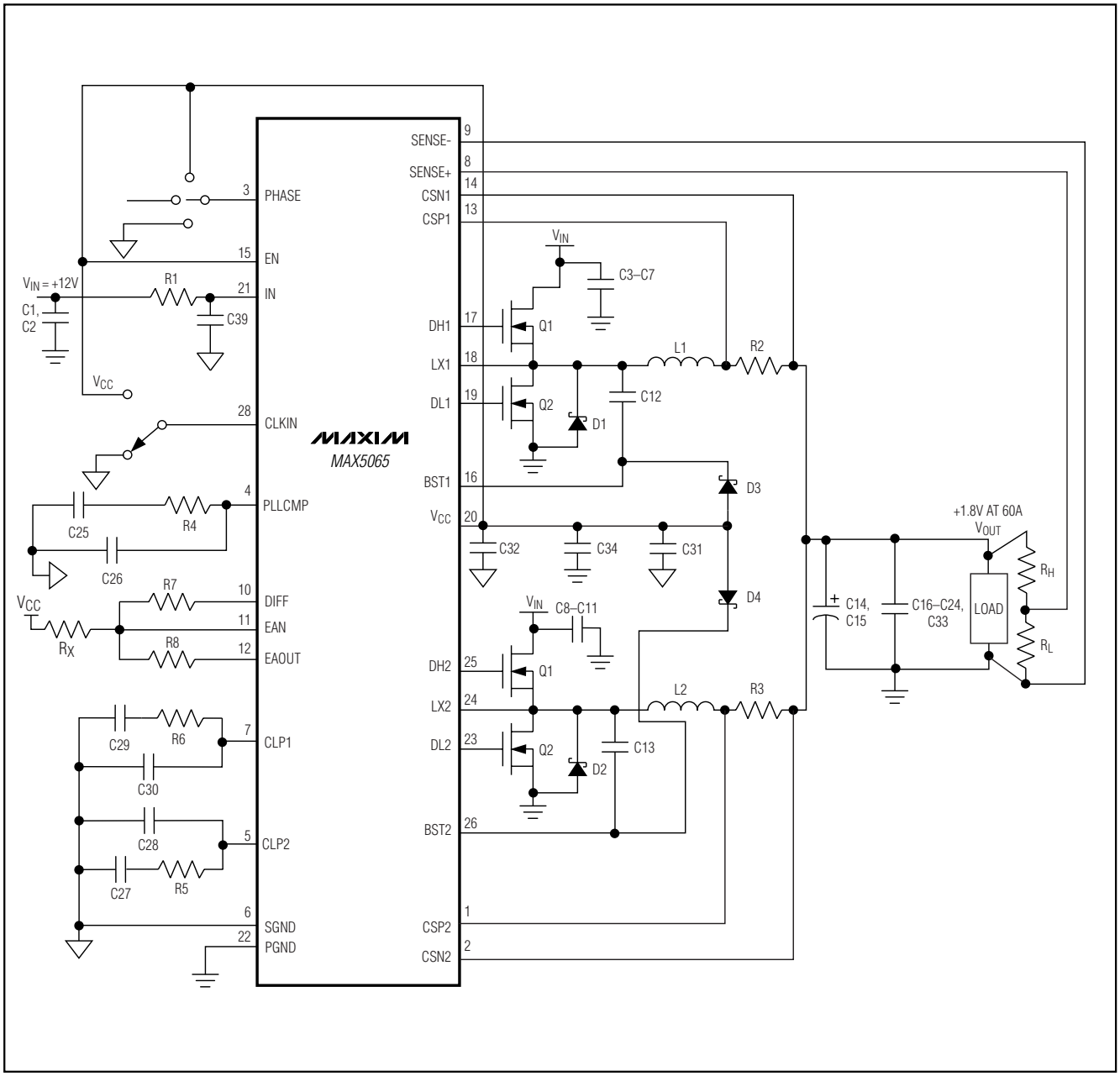


Figure 3. MAX5065 Typical Application Circuit

where, Q_{G1}, Q_{G2}, Q_{G3}, and Q_{G4} are the total gate charge of the low-side and high-side external MOSFETs, I_Q is 4mA (typ), and f_{SW} is the switching frequency of each individual phase.

For applications utilizing a +5V input voltage, disable the V_{CC} regulator by connecting IN and V_{CC} together.

Undervoltage Lockout (UVLO)/Soft-Start

The MAX5065/MAX5067 include an undervoltage lockout with hysteresis and a power-on reset circuit for converter turn-on and monotonic rise of the output voltage. The UVLO threshold is internally set between +4.0V and +4.5V with a 200mV hysteresis. Hysteresis at UVLO eliminates "chattering" during startup.

Most of the internal circuitry, including the oscillator, turns on when the input voltage reaches +4V. The MAX5065/MAX5067 draw up to 4mA of current before the input voltage reaches the UVLO threshold.

The compensation network at the current-error amplifiers (CLP1 and CLP2) provides an inherent soft-start of the output voltage. It includes a parallel combination of capacitors (C34, C36) and resistors (R5, R6) in series with other capacitors (C33, C35) (see Figures 1 and 2). The voltage at CLP_ limits the maximum current available to charge output capacitors. The capacitor on CLP_ in conjunction with the finite output-drive current of the current-error amplifier yields a finite rise time for the output current and thus the output voltage.

Internal Oscillator

The internal oscillator generates the 180° out-of-phase clock signals required by the pulse-width modulation (PWM) circuits. The oscillator also generates the $2V_{P-P}$ voltage ramp signals necessary for the PWM comparators. Connect CLKIN to SGND to set the internal oscillator frequency to 250kHz or connect CLKIN to V_{CC} to set the internal oscillator to 500kHz.

CLKIN is a CMOS logic clock input for the phase-locked loop (PLL). When driven externally, the internal oscillator locks to the signal at CLKIN. A rising edge at CLKIN starts the ON cycle of the PWM. Ensure that the external clock pulse width is at least 200ns. CLKOUT provides a phase-shifted output with respect to the rising edge of the signal at CLKIN. PHASE sets the amount of phase shift at CLKOUT. Connect PHASE to V_{CC} for 120° of phase shift, leave PHASE unconnected for 90° of phase shift, or connect PHASE to SGND for 60° of phase shift with respect to CLKIN.

The MAX5065/MAX5067 require compensation on PLLCMP even when operating from the internal oscillator. The device requires an active PLL to generate the proper clock signal required for PWM operation.

Control Loop

The MAX5065/MAX5067 use an average-current-mode control scheme to regulate the output voltage (Figure 4). The main control loop consists of an inner current loop and an outer voltage loop. The inner loop controls the output currents (I_{PHASE1} and I_{PHASE2}) while the outer loop controls the output voltage. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a singlepole system.

The current loop consists of a current-sense resistor (R_S), a current-sense amplifier (CA_), a current-error amplifier (CEA_), an oscillator providing the carrier ramp, and a PWM comparator (CPWM_). The precision CA_ amplifies the sense voltage across R_S by a factor of 18. The inverting input to the CEA_ senses the CA_ output. The CEA_ output is the difference between the voltage-error amplifier output (EAOUT) and the gained-up voltage from the CA_. The RC compensation network connected to CLP1 and CLP2 provides external frequency compensation for the respective CEA_. The start of every clock cycle enables the high-side drivers and initiates a PWM ON cycle. Comparator CPWM_ compares the output voltage from the CEA_ with a 0 to +2V ramp from the oscillator. The PWM ON cycle terminates when the ramp voltage exceeds the error voltage.

The outer voltage control loop consists of the differential amplifier (DIFF AMP), reference voltage, and VEA. The unity-gain differential amplifier provides true differential remote sensing of the output voltage. The differential amplifier output connects to the inverting input (EAN) of the VEA. The noninverting input of the VEA is internally connected to an internal precision reference voltage. The MAX5067 reference voltage is set to +0.8V and the MAX5065 reference is set to +0.6V. The VEA controls the two inner current loops (Figure 4). Use a resistive feedback network to set the VEA gain as required by the adaptive voltage-positioning circuit (see the *Adaptive Voltage Positioning* section).

Current-Sense Amplifier

The differential current-sense amplifier (CA_) provides a DC gain of 18. The maximum input offset voltage of the current-sense amplifier is 1mV and the common-mode voltage range is -0.3V to +3.6V. The current-sense amplifier senses the voltage across a current-sense resistor.

Peak-Current Comparator

The peak-current comparator provides a path for fast cycle-by-cycle current limit during extreme fault conditions such as an output inductor malfunction (Figure 5). Note that the average current-limit threshold of 48mV still limits the output current during short-circuit conditions. To prevent inductor saturation, select an output

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

inductor with a saturation current specification greater than the average current limit (48mV). Proper inductor selection ensures that only extreme conditions trip the peak-current comparator, such as a cracked output inductor. The 112mV voltage threshold for triggering the peak-current limit is twice the full-scale average current-limit voltage threshold. The peak-current comparator has a delay of only 260ns.

Current-Error Amplifier

Each phase of the MAX5065/MAX5067 has a dedicated transconductance current-error amplifier (CEA_) with a typical g_m of 550µS and 320µA output sink and source current capability. The current-error amplifier outputs, CLP1 and CLP2, serve as the inverting input to the PWM comparator. CLP1 and CLP2 are externally accessible to provide frequency compensation for the inner current loops (Figure 4). Compensate CEA_ so the inductor current down slope, which becomes the up slope to the inverting input of the PWM comparator, is less than the slope of the internally generated voltage ramp (see the *Compensation* section).

PWM Comparator and R-S Flip-Flop

The PWM comparator (CPWM) sets the duty cycle for each cycle by comparing the output of the current-error amplifier to a $2V_{P-P}$ ramp. At the start of each clock cycle, an R-S flip-flop resets and the high-side driver (DH_) turns on. The comparator sets the flip-flop as soon as the ramp voltage exceeds the CLP_ voltage, thus terminating the ON cycle (Figure 5).

Differential Amplifier

The differential amplifier (DIFF AMP) facilitates output voltage remote sensing at the load (Figure 4). It provides true differential output voltage sensing while rejecting the common-mode voltage errors due to high-current ground paths. Sensing the output voltage

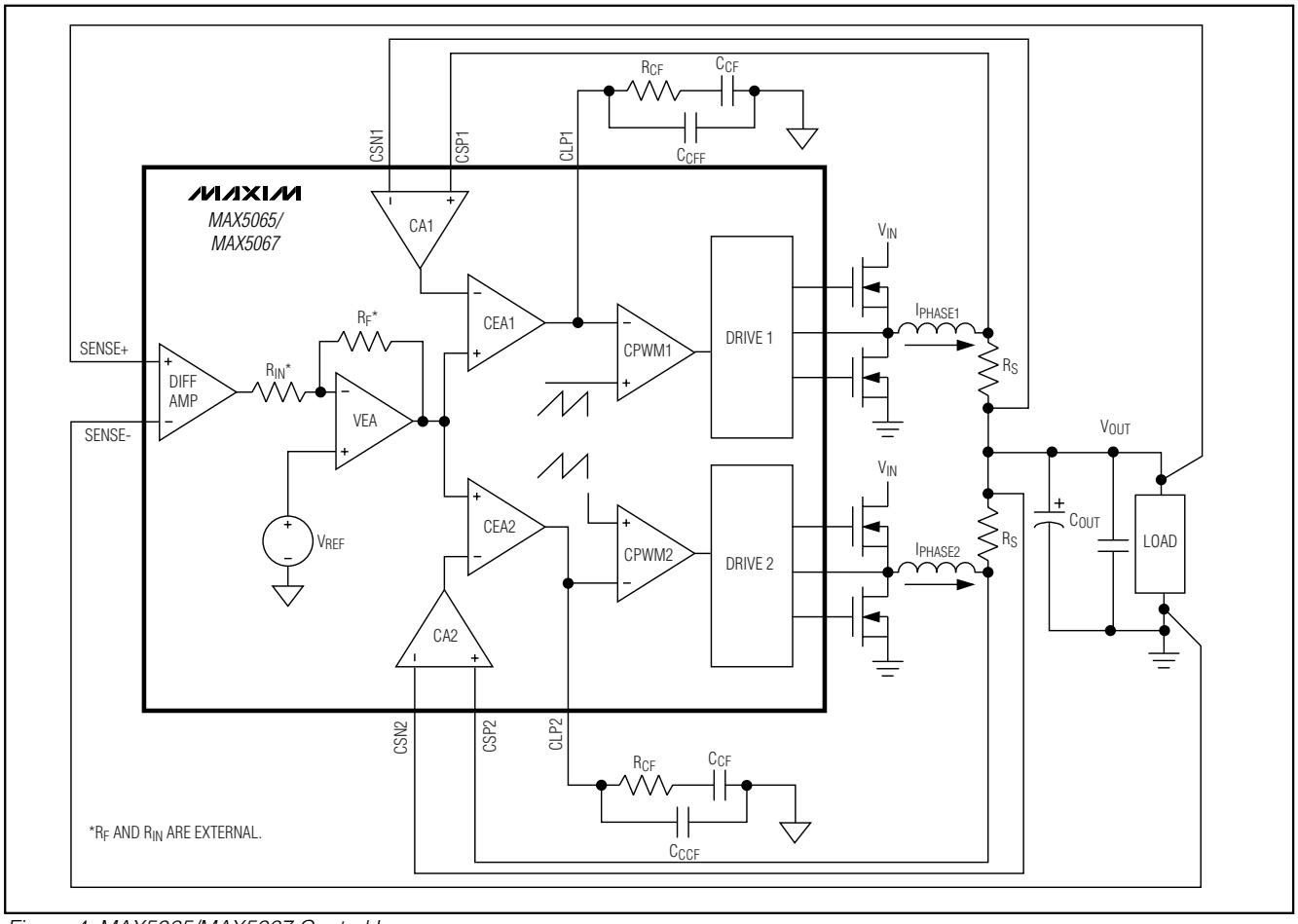


Figure 4. MAX5065/MAX5067 Control Loop

directly at the load provides accurate load voltage sensing in high-current environments. The VEA provides the difference between the differential amplifier output (DIFF) and the desired output voltage. The differential amplifier has a bandwidth of 3MHz. The difference between SENSE+ and SENSE- regulates to +0.6V for the MAX5065 and regulates to +0.8V for the MAX5067. Connect SENSE+ to the center of the resistive-divider from the output to SENSE-.

Voltage-Error Amplifier

The VEA sets the gain of the voltage control loop and determines the error between the differential amplifier output and the internal reference voltage (V_{REF}).

The VEA output clamps to +0.9V relative to V_{CM} (+0.6V), thus limiting the average maximum current from individual phases. The maximum average current-limit threshold for each phase is equal to the maximum clamp voltage of the VEA divided by the gain (18) of the current-sense amplifier. This results in accurate settings for the average maximum current for each phase. Set the VEA gain using R_F and R_{IN} for the amount of output voltage positioning required within the rated current range as discussed in the *Adaptive Voltage Positioning* section (Figure 4).

$$V_{OUT(NL)} = \left(1+\frac{R_{IN}}{R_F}\right)\times\left(\frac{R_H+R_L}{R_L}\right)\times V_{REF} \quad (3)$$

where R_H and R_L are the feedback resistor network (Figures 1, 2). V_{REF} = 0.6V (MAX5065) or 0.8V (MAX5067).

Some applications require V_{OUT} equal to $V_{OUT(NOM)}$ at no load. To ensure that the output voltage does not exceed the nominal output voltage ($V_{OUT(NOM)}$), add a resistor R_X from V_{CC} to EAN.

Use the following equations to calculate the value of R_X.

For MAX5065:

$$R_X = [V_{CC} - 1.2]\times\frac{R_F}{0.6V} \quad (4)$$

For MAX5067:

$$R_X = [V_{CC} - 1.4]\times\frac{R_F}{0.8V} \quad (5)$$

Adaptive Voltage Positioning

Powering new-generation processors requires new techniques to reduce cost, size, and power dissipation. Voltage positioning reduces the total number of output capacitors to meet a given transient response requirement. Setting the no-load output voltage slightly higher than the output voltage during nominally loaded conditions allows a larger downward voltage excursion when the output current suddenly increases. Regulating at a lower output voltage under a heavy load allows a larger upward-voltage excursion when the output current suddenly decreases. A larger allowed, voltage-step excursion reduces the required number of output capacitors

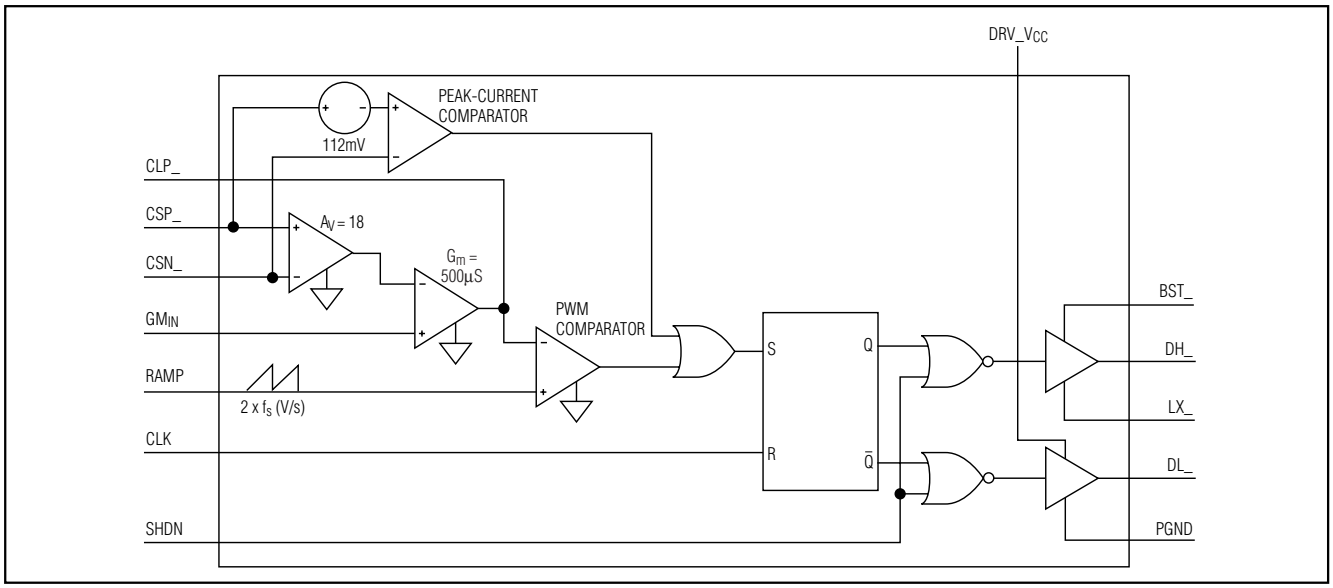


Figure 5. Phase Circuit (Phase 1/Phase 2)

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

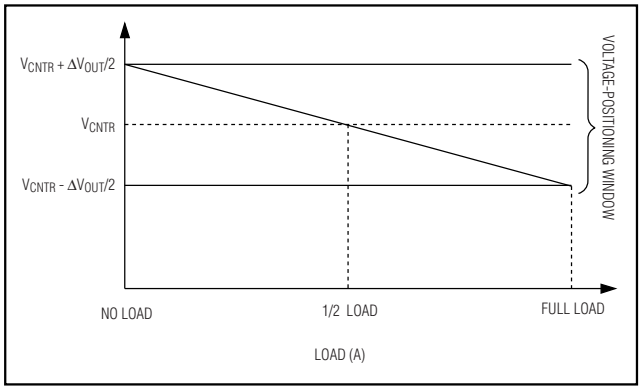


Figure 6. Defining the Voltage-Positioning Window

or allows for the use of higher ESR capacitors.

Voltage positioning may require the output to regulate away from a center value. Define the center value as the voltage where the output drops ($\Delta V_{OUT}/2$) at one half the maximum output current (Figure 6).

Set the voltage-positioning window (ΔV_{OUT}) using the resistive feedback of the VEA. Use the following equations to calculate the voltage-positioning window for the MAX5065/MAX5067:

$$\Delta V_{OUT} = \frac{I_{OUT} \times R_{IN}}{2 \times G_C \times R_F} \times \frac{R_H + R_L}{R_L} \quad (6)$$

$$G_C = \frac{0.05}{R_S} \quad (7)$$

where R_{IN} and R_F are the input and feedback resistors of the VEA, G_C is the current-loop transconductance, and R_S is the current-sense resistor.

Phase-Locked Loop: Operation and Compensation

The PLL synchronizes the internal oscillator to the external frequency source when driving CLKIN. Connecting CLKIN to V_{CC} or SGND forces the PWM frequency to default to the internal oscillator frequency of 500kHz or 250kHz, respectively. The PLL uses a conventional architecture consisting of a phase detector and a charge pump capable of providing 20µA of output current. Connect an external series combination capacitor (C31) and resistor (R4) and a parallel capacitor (C32) from PLLCMP to SGND to provide frequency compensation for the PLL (Figure 1). The pole-zero pair compensation provides a zero defined by 1 / [R4 x (C31 + C32)] and a pole defined by 1 / (R4 x C32). Use the following typical values for compensating the PLL:

R4 = 7.5kΩ, C31 = 4.7nF, C32 = 470pF. If changing the PLL frequency, expect a finite locking time of approximately 200µs.

The MAX5065/MAX5067 require compensation on PLLCMP even when operating from the internal oscillator. The device requires an active PLL in order to generate the proper internal PWM clocks.

MOSFET Gate Drivers (DH_, DL_)

The high-side (DH_) and low-side (DL_) drivers drive the gates of external N-channel MOSFETs (Figures 1, 2, and 3). The drivers' high-peak sink and source current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced cross-conduction losses. For modern CPU voltage-regulating module applications where the duty cycle is less than 50%, choose high-side MOSFETs (Q1 and Q3) with a moderate $R_{DS(ON)}$ and a very low gate charge. Choose low-side MOSFETs (Q2 and Q4) with very low $R_{DS(ON)}$ and moderate gate charge.

The driver block also includes a logic circuit that provides an adaptive nonoverlap time to prevent shoot-through currents during transition. The typical nonoverlap time is 60ns between the high-side and low-side MOSFETs.

BST_

The MAX5067 uses V_{DD} to power the low- and high-side MOSFET drivers. The high-side drivers derive their power through a bootstrap capacitor and V_{DD} supplies power internally to the low-side drivers. Connect a 0.47µF low-ESR ceramic capacitor between BST_ and LX_. Bypass V_{CC} to SGND with 4.7µF and 0.1µF low-ESR ceramic capacitors in parallel. Reduce the PC board area formed by these capacitors, the rectifier diodes between V_{CC} and the boost capacitor, the MAX5065/MAX5067, and the switching MOSFETs.

Overload Conditions

Average-current-mode control has the ability to limit the average current sourced by the converter during a fault condition. When a fault condition occurs, the VEA output clamps to +0.9V with respect to the common-mode voltage (V_{CM} = +0.6V) and is compared with the output of the current-sense amplifiers (CA1 and CA2) (see Figure 4). The current-sense amplifier's gain of 18 limits the maximum current in the inductor or sense resistor to $I_{LIMIT} = 50mV/R_S$.

Protection

The MAX5067 includes output overvoltage protection (OVP), undervoltage protection (UVP), phase failure, and overload protection to prevent damage to the powered electronic circuits.

Overvoltage Protection (MAX5067)

The OVP comparator compares the OVPIN input to the overvoltage threshold (Figure 7). The overvoltage threshold is typically +0.8V. A detected overvoltage event latches the comparator output forcing the power stage into the OVP state. In the OVP state, the high-side MOSFETs turn off and the low-side MOSFETs latch on. Use the OVPOUT high-current output driver to turn on an external crowbar SCR. When the crowbar SCR turns on, a fuse must blow or the source current for the MAX5067 regulator must be limited to prevent further damage to the external circuitry. Connect the SCR close to the input source and after the fuse. Use an SCR large enough to handle the peak I^2t energy due to the input and output capacitors discharging and the current sourced by the power-source output. Connect DIFF to OVPIN for differential output sensing and overvoltage protection. Add an RC delay to reduce the sensitivity of the overvoltage circuit and avoid nuisance tripping of the converter (Figures 1, 2). Connect a resistor-divider from the load to SGND to set the OVP output voltage.

$$V_{OVP} = \left(1 + \frac{R_A}{R_B}\right) \times 0.8V \qquad (8)$$

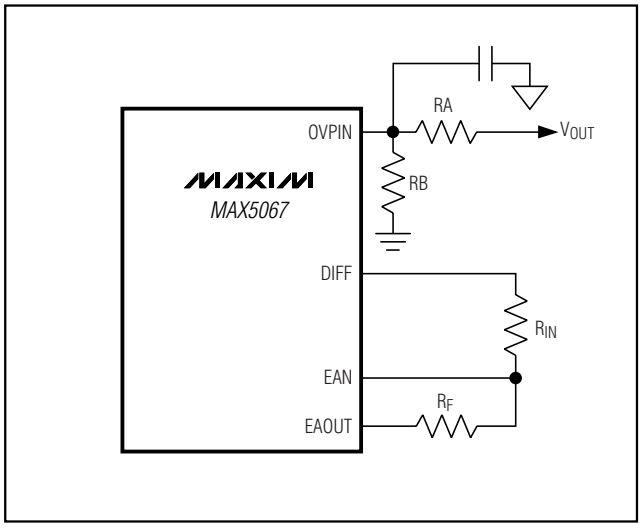


Figure 7. OVP Input Delay

Power-Good Generator (MAX5067)

The PGOOD output is high if all of the following conditions are met (Figure 8):

1) The output is within 90% to 108% of the programmed output voltage.
2) Both phases are providing current.
3) EN is high.

A window comparator compares the differential amplifier output (DIFF) against 1.08 times the set output voltage for overvoltage and 0.90 times the set output voltage for undervoltage monitoring. The phase-failure comparator detects a phase failure by comparing the current-error-amplifier output (CLP_) with a 2.0V reference.

Use a 10kΩ pullup resistor from PGOOD to a voltage source less than or equal to V_{CC}. An output voltage outside the comparator window or a phase-failure condition forces the open-drain output low. The open-drain MOSFET sinks 4mA of current while maintaining less than 0.2V at the PGOOD output.

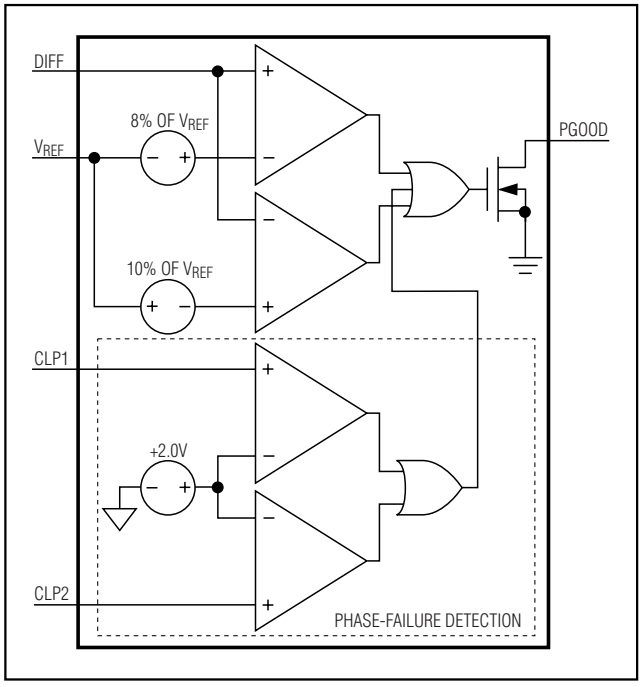


Figure 8. Power-Good Generator (MAX5067)

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

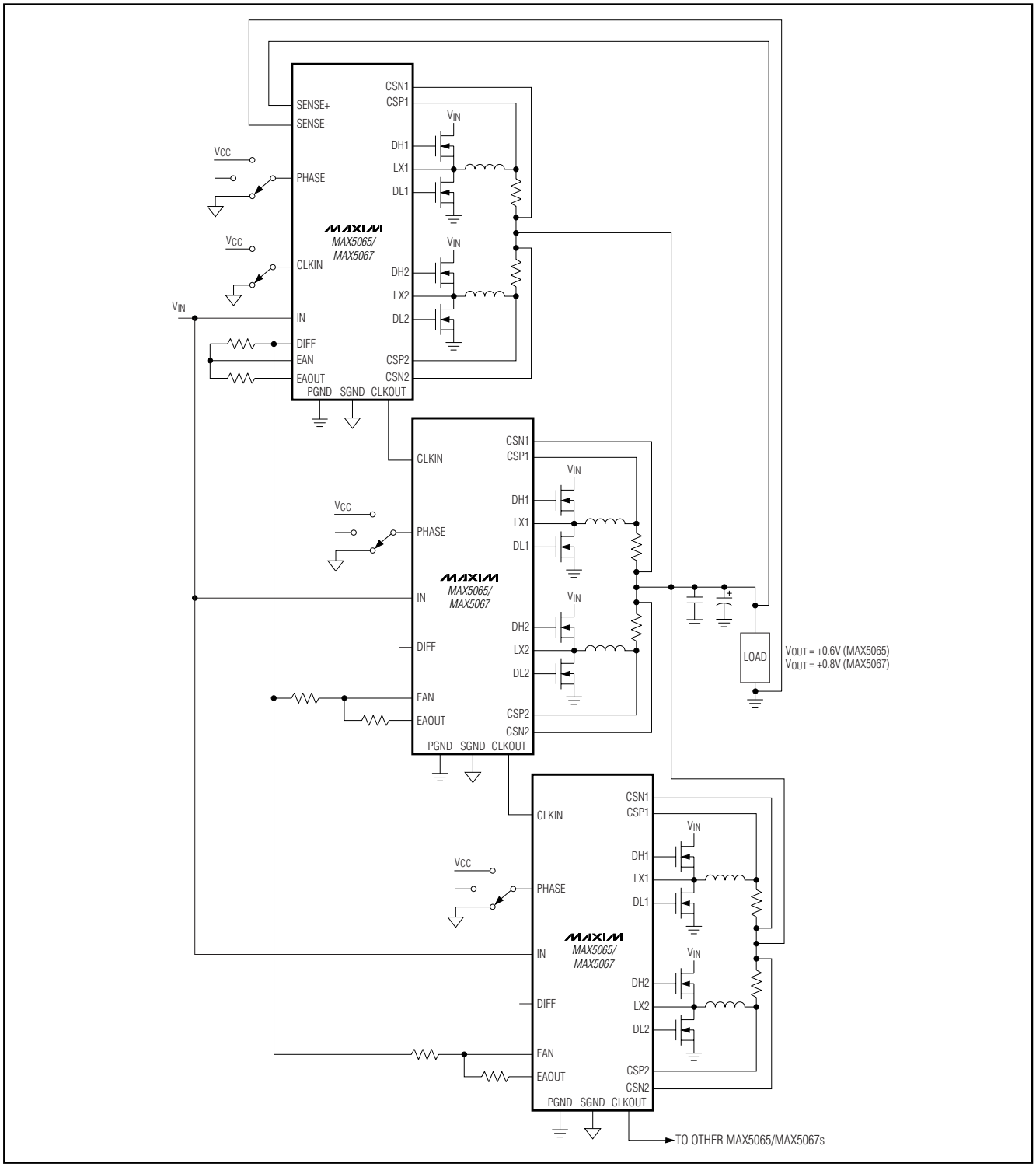


Figure 9. Parallel Configuration of Multiple MAX5065/MAX5067s

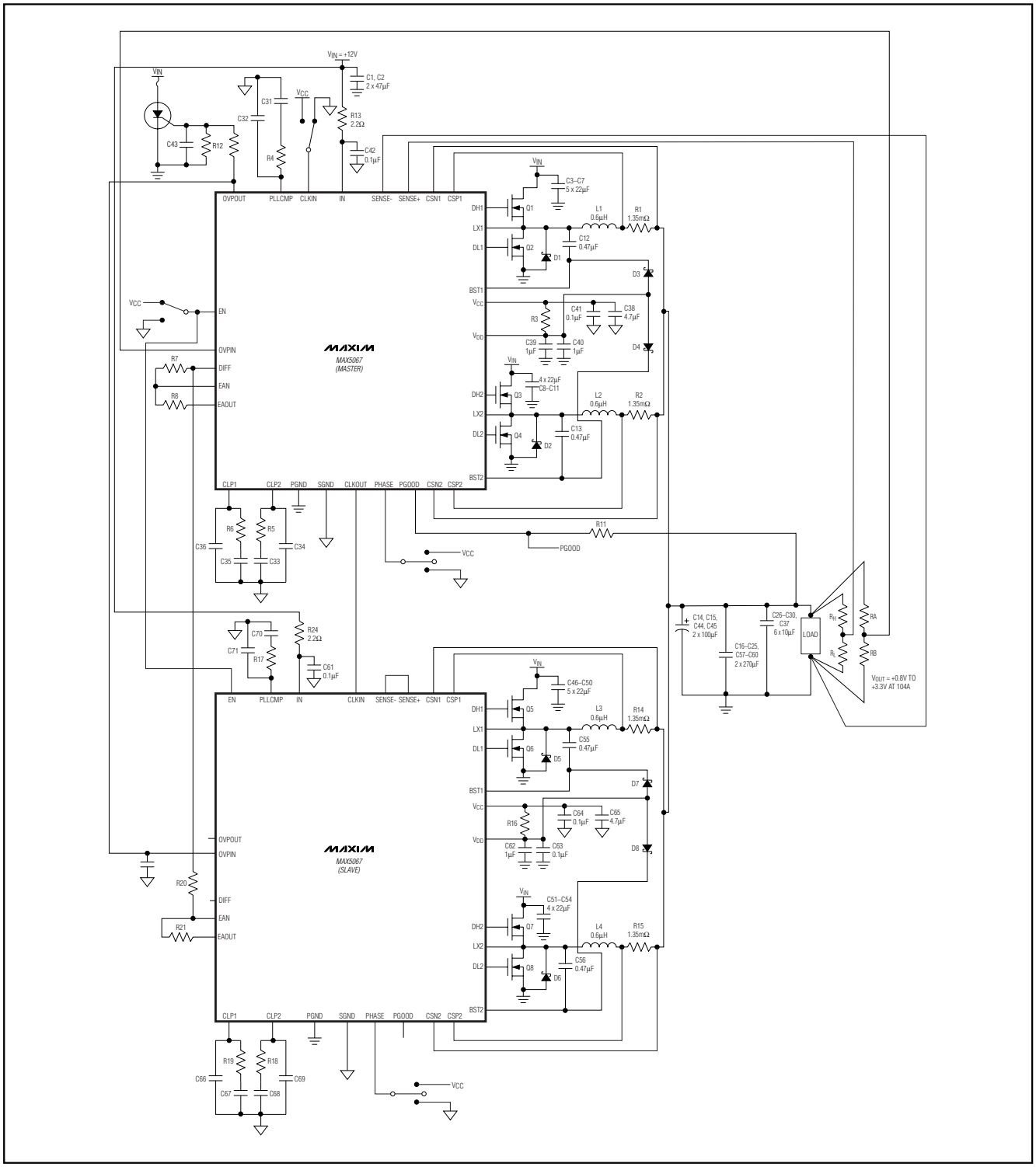


Figure 10. Four-Phase Parallel Application Circuit (V_{IN} = +12V, V_{OUT} = +0.8V to +3.3V at 104A)

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

Phase-Failure Detector (MAX5067)

Output current contributions from the two phases are within ±10% of each other. Proper current sharing reduces the necessity to overcompensate the external components. However, an undetected failure of one phase driver causes the other phase driver to run continuously as it tries to provide the entire current requirement to the load. Eventually, the stressed operational phase driver fails.

During normal operating conditions, the voltage level on CLP_ is within the peak-to-peak voltage levels of the PWM ramp. If one of the phases fails, the control loop raises the CLP_ voltage above its operating range. To determine a phase failure, the phase-failure detection circuit (Figure 8) monitors the output of the current amplifiers (CLP1 and CLP2) and compares them to a 2.0V reference. If the voltage levels on CLP1 or CLP2 are above the reference level for more than 1250 clock cycles, the phase failure circuit forces PGOOD low.

Parallel Operation

For applications requiring large output current, parallel up to three MAX5065/MAX5067s (six phases) to triple the available output current (see Figures 9 and 10). The paralleled converters operate at the same switching frequency but different phases keep the capacitor ripple RMS currents to a minimum. Three parallel MAX5065/MAX5067 converters deliver up to 180A of output current. To set the phase shift of the on-board PLL, leave PHASE unconnected for 90° of phase shift (2 paralleled converters), or connect PHASE to SGND for 60° of phase shift (3 converters in parallel). Designate one converter as master and the remaining converters as slaves. Connect the master and slave controllers in a daisy-chain configuration as shown in Figure 9. Connect CLKOUT from the master controller to CLKIN of the first slaved controller, and CLKOUT from the first slaved controller to CLKIN of the second slaved controller. Choose the appropriate phase shift for minimum ripple currents at the input and output capacitors. The master controller senses the output differential voltage through SENSE+ and SENSE- and generates the DIFF voltage. Disable the voltage sensing of the slaved controllers by leaving DIFF unconnected (floating). Figure 10 shows a detailed typical parallel application circuit using two MAX5067s. This circuit provides four phases at an input voltage of +12V and an output voltage range of +0.6V to +3.3V (MAX5065) and +0.8V to +3.3V (MAX5067) at 104A.

Applications Information

Each MAX5065/MAX5067 circuit drives two 180° out-of-phase channels. Parallel two or three MAX5065/MAX5067 circuits to achieve four- or six-phase operation, respectively. Figure 1 shows the typical application circuit for a two-phase operation. The design criteria for a two-phase converter includes frequency selection, inductor value, input/output capacitance, switching MOSFETs, sense resistors, and the compensation network. Follow the same procedure for the four- and six-phase converter design, except for the input and output capacitance. The input and output capacitance requirements vary depending on the operating duty cycle.

The examples discussed in this data sheet pertain to a typical application with the following specifications:

V_{IN} = +12V

V_{OUT} = +1.8V

$I_{OUT(MAX)}$ = 52A

f_{SW} = 250kHz

Peak-to-Peak Inductor Current (ΔI_L) = 10A

Table 1 shows a list of recommended external components (Figure 1) and Table 2 provides component supplier information.

Number of Phases

Selecting the number of phases for a voltage regulator depends mainly on the ratio of input-to-output voltage (operating duty cycle). Optimum output-ripple cancellation depends on the right combination of operating duty cycle and the number of phases. Use the following equation as a starting point to choose the number of phases:

$$N_{PH} \approx K/D \quad (9)$$

where K = 1, 2, or 3 and the duty cycle is $D = V_{OUT}/V_{IN}$.

Choose K to make N_{PH} an integer number. For example, converting V_{IN} = +12V to V_{OUT} = +1.8V yields better ripple cancellation in the six-phase converter than in the four-phase converter. Ensure that the output load justifies the greater number of components for multiphase conversion. Generally limiting the maximum output current to 25A per phase yields the most cost-effective solution. The maximum ripple cancellation occurs when $N_{PH} = K/D$.

Single-phase conversion requires greater size and power dissipation for external components such as the switching MOSFETs and the inductor. Multiphase conversion eliminates the heatsink by distributing the power dissipation in the external components. The multiple phases operating at given phase shifts effectively increase the switching frequency seen by the input/output capacitors, thereby reducing the input/output capacitance requirement for the same ripple performance. The lower inductance value improves the large-signal response of the converter during a transient load at the output. Consider

Table 1. Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2	2	47µF,16V X5R input-filter capacitors TDK C5750X5R1C476M
C3–C11	9	22µF, 16V input-filter capacitors TDK C4532X5R1C226M
C12, C13	2	0.47µF, 16V capacitors TDK C1608X5R1A474K
C14, C15	2	100µF, 6.3V, output-filter capacitors Murata GRM44-1X5R107K6.3
C16–C25	10	270µF, 2V output-filter capacitors Panasonic EEFUE0D271R
C26–C30, C37	6	10µF, 6.3V output-filter capacitors TDK C2012X5R05106M
C31	1	4700pF, 16V X7R capacitor Vishay-Siliconix VJ0603Y471JXJ
C32, C34, C36	3	470pF, 16V capacitors Murata GRM1885C1H471JAB01
C33, C35, C43	3	0.01µF, 50V X7R capacitors Murata GRM188R71H103KA01
C38	1	4.7µF, 16V X5R capacitor Murata GRM40-034X5R475k6.3
C39	1	0.1µF, 10V Y5V capacitor Murata GRM188F51A105
C40, C41, C42	3	0.1µF, 16V X7R capacitors Murata GRM188R71C104KA01
C44	1	100pF—OVPIN capacitor
D1, D2	2	Schottky diodes ON-Semiconductor MBRS340T3
D3, D4	2	Schottky diodes ON-Semiconductor MBR0520LT1
L1, L2	2	0.6µH, 27A inductors Panasonic ETQP1H0R6BFX
Q1, Q3	2	Upper-power MOSFETs Vishay-Siliconix Si7860DP
Q2, Q4	2	Lower-power MOSFETs Vishay-Siliconix Si7886DP
R1, R2	4	Current-sense resistors, use two 2.7mΩ resistors in parallel, Panasonic ERJM1WSF2M7U
R3, R13	2	2.2Ω ±1% resistors
R4	2	7.5kΩ ±1% resistor
R5, R6	2	1kΩ ±1% resistors
R_{IN}	1	4.99kΩ ±1% resistor
R_f	1	37.4kΩ ±1% resistor
R11	1	10kΩ ±1% resistor
R12	1	10kΩ ±1% resistor
RA	1	See the *Overvoltage Protection (MAX5067)* section
RB	1	See the *Overvoltage Protection (MAX5067)* section
RH	1	See the *Adaptive Voltage Positioning and Voltage-Error Amplifier* sections
RL	1	See the *Adaptive Voltage Positioning and Voltage-Error Amplifier* sections
RX	1	Open circuit

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Murata	770-436-1300	770-436-3030	www.murata.com
ON Semiconductor	602-244-6600	602-244-3345	www.on-semi.com
Panasonic	714-373-7939	714-373-7183	www.panasonic.com
TDK	847-803-6100	847-390-4405	www.tcs.tdk.com
Vishay-Siliconix	1-800-551-6933	619-474-8920	www.vishay.com

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

all these issues when determining the number of phases necessary for the voltage regulator application.

Inductor Selection

The switching frequency per phase, peak-to-peak ripple current in each phase, and allowable ripple at the output determine the inductance value.

Selecting higher switching frequencies reduces the inductance requirement, but at the cost of lower efficiency. The charge/discharge cycle of the gate and drain capacitances in the switching MOSFETs create switching losses. The situation worsens at higher input voltages, since switching losses are proportional to the square of input voltage. Use 500kHz per phase for V_{IN} = +5V and 250kHz or less per phase for $V_{IN} \geq$ +12V.

Although lower switching frequencies per phase increase the peak-to-peak inductor ripple current (ΔI_L), the ripple cancellation in the multiphase topology reduces the input and output capacitor RMS ripple current.

Use the following equation to determine the minimum inductance value:

$$L_{MIN} = \frac{(V_{INMAX} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times \Delta I_L} \qquad (10)$$

Choose ΔI_L equal to about 40% of the output current per phase. Since ΔI_L affects the output-ripple voltage, the inductance value may need minor adjustment after choosing the output capacitors for full-rated efficiency.

Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. Particular applications may require custom-made inductors. Use high-frequency core material for custom inductors. High ΔI_L causes large peak-to-peak flux excursion increasing the core losses at higher frequencies. The high-frequency operation coupled with high ΔI_L, reduces the required minimum inductance and even makes the use of planar inductors possible. The advantages of using planar magnetics include low-profile design, excellent current-sharing between phases due to the tight control of parasitics, and low cost.

For example, calculate the minimum inductance at $V_{IN(MAX)}$ = +13.2V, V_{OUT} = +1.8V, ΔI_L = 10A, and f_{SW} = 250kHz:

$$L_{MIN} = \frac{(13.2 - 1.8) \times 1.8}{13.2 \times 250k \times 10} = 0.6\mu H \qquad (11)$$

The average-current-mode control feature of the MAX5065/MAX5067 limits the maximum peak inductor current and prevents the inductor from saturating. Choose an inductor with a saturating current greater than the worst-case peak inductor current. Use the following equation to determine the worst-case inductor current for each phase:

$$I_{L\_PEAK} = \frac{0.051V}{R_{SENSE}} + \frac{\Delta I_L}{2} \qquad (12)$$

where R_{SENSE} is the sense resistor in each phase.

Switching MOSFETs

When choosing a MOSFET for voltage regulators, consider the total gate charge, $R_{DS(ON)}$, power dissipation, and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications.

The average gate-drive current from the MAX5065/MAX5067 output is proportional to the total capacitance it drives from DH1, DH2, DL1, and DL2. The power dissipated in the MAX5065/MAX5067 is proportional to the input voltage and the average drive current. See the *V_{IN}, V_{CC}, V_{DD}* section to determine the maximum total gate charge allowed from all the driver outputs combined.

The gate charge and drain capacitance ($CV^{2)}$ loss, the cross-conduction loss in the upper MOSFET due to finite rise/fall time, and the I^2R loss due to RMS current in the MOSFET $R_{DS(ON)}$ account for the total losses in the MOSFET. Estimate the power loss ($PD_{MOS\_}$) in the high-side and low-side MOSFETs using the following equations:

$$PD_{MOS-HI} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{4}\right) + 1.4R_{DS(ON)} \times I^2_{RMS-HI} \qquad (13)$$

where Q_G, $R_{DS(ON)}$, t_R, and t_F are the upper-switching MOSFET's total gate charge, on-resistance at +25°C, rise time, and fall time, respectively.

$$I_{RMS-HI} = \sqrt{\left(I^2_{DC} + I^2_{PK} + I_{DC} \times I_{PK}\right) \times \frac{D}{3}} \qquad (14)$$

where $D = V_{OUT}/V_{IN}$, $I_{DC} = (I_{OUT} - \Delta I_L)/2$ and $I_{PK} = (I_{OUT} + \Delta I_L)/2$

$$PD_{MOS-LO} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{2 \times C_{OSS} \times V_{IN}^2 \times f_{SW}}{3}\right) + 1.4R_{DS(ON)} \times I^2_{RMS-LO} \quad (15)$$

where C_{OSS} is the MOSFET drain-to-source capacitance.

$$I_{RMS-LO} = \sqrt{\left(I^2_{DC} + I^2_{PK} + I_{DC} \times I_{PK}\right) \times \frac{(1-D)}{3}} \quad (16)$$

For example, from the typical specifications in the *Applications Information* section with V_{OUT} = +1.8V, the high-side and low-side MOSFET RMS currents are 9.9A and 24.1A, respectively. Ensure that the thermal impedance of the MOSFET package keeps the junction temperature at least 25°C below the absolute maximum rating. Use the following equation to calculate maximum junction temperature:

$$T_J = PD_{MOS} \times \theta_{J-A} + T_A \quad (17)$$

Table 3. Peak-to-Peak Output Ripple Current Calculations

NUMBER OF PHASES (N)	DUTY CYCLE (D)	EQUATION FOR ΔI_{P-P}
2	< 50%	$\Delta I = \frac{V_O(1-2D)}{L \times f_{SW}}$
2	> 50%	$\Delta I = \frac{(V_{IN} - V_O)(2D-1)}{L \times f_{SW}}$
4	0 to 25%	$\Delta I = \frac{V_O(1-4D)}{L \times f_{SW}}$
4	25% to 50%	$\Delta I = \frac{V_O(1-2D)(4D-1)}{2 \times D \times L \times f_{SW}}$
4	> 50%	$\Delta I = \frac{V_O(2D-1)(3-4D)}{D \times L \times f_{SW}}$
6	< 17%	$\Delta I = \frac{V_O(1-6D)}{L \times f_{SW}}$

Input Capacitors

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. Increasing the number of phases increases the effective switching frequency and lowers the peak-to-average current ratio, yielding a lower input capacitance requirement.

The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high-ripple-current capability at the input. Assume the contributions from the ESR and capacitor discharge are equal to 30% and 70%, respectively. Calculate the input capacitance and ESR required for a specified ripple using the following equation:

$$ESR_{IN} = \frac{(\Delta V_{ESR})}{\left(\frac{I_{OUT}}{N} + \frac{\Delta I_L}{2}\right)} \quad (18)$$

$$C_{IN} = \frac{\frac{I_{OUT}}{N} \times D(1-D)}{\Delta V_Q \times f_{SW}} \quad (19)$$

where I_{OUT} is the total output current of the multiphase converter and N is the number of phases.

For example, at V_{OUT} = +1.8V, the ESR and input capacitance are calculated for the input peak-to-peak ripple of 100mV or less yielding an ESR and capacitance value of 1mΩ and 200µF.

Output Capacitors

The worst-case peak-to-peak and capacitor RMS ripple current, the allowable peak-to-peak output ripple voltage, and the maximum deviation of the output voltage during step loads determine the capacitance and the ESR requirements for the output capacitors.

In multiphase converter design, the ripple currents from the individual phases cancel each other and lower the ripple current. The degree of ripple cancellation depends on the operating duty cycle and the number of phases. Choose the right equation from Table 3 to calculate the peak-to-peak output ripple (ΔI_{P-P}) for a given duty cycle of two-, four-, and six-phase converters. The maximum ripple cancellation occurs when N_{PH} = K / D.

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

The allowable deviation of the output voltage during the fast transient load dictates the output capacitance and ESR. The output capacitors supply the load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The resistive drop across the capacitor ESR and capacitor discharge causes a voltage drop during a step load. Use a combination of SP polymer and ceramic capacitors for better transient load and ripple/noise performance.

Keep the maximum output voltage deviation less than or equal to the adaptive voltage-positioning window (ΔV_{OUT}). Assume 50% contribution each from the output capacitance discharge and the ESR drop. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}} \quad (20)$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q} \quad (21)$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the controller. Controller response time depends on the control-loop bandwidth.

Current Limit

The average-current-mode control technique of the MAX5065/MAX5067 accurately limits the maximum output current per phase. The MAX5065/MAX5067 sense the voltage across the sense resistor and limit the peak inductor current ($I_{L\text{-}PK}$) accordingly. The ON cycle terminates when the current-sense voltage reaches 45mV (min). Use the following equation to calculate maximum current-sense resistor value:

$$R_{SENSE} = \frac{0.045}{\frac{I_{OUT}}{N}} \quad (22)$$

$$PD_R = \frac{2.5 \times 10^{-3}}{R_{SENSE}} \quad (23)$$

where PD_R is the power dissipation in sense resistors. Select 5% lower value of R_{SENSE} to compensate for any parasitics associated with the PC board. Also, select a non inductive resistor with the appropriate wattage rating.

Reverse Current Limit

The MAX5065/MAX5067 limit the reverse current when V_{BUS} is higher than the preset output voltage.

Calculate the maximum reverse current based on V_{CLR}, the reverse-current-limit threshold, and the current-sense resistor.

$$I_{REVERSE} = \frac{2 \times V_{CLR}}{R_{SENSE}} \quad (24)$$

where $I_{REVERSE}$ is the total reverse current into the converter.

Compensation

The main control loop consists of an inner current loop and an outer voltage loop. The MAX5065/MAX5067 use an average-current-mode control scheme to regulate the output voltage (Figure 4). I_{PHASE1} and I_{PHASE2} are the inner average current loops. The VEA output provides the controlling voltage for these current sources. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

A resistive feedback around the VEA provides the best possible response, since there are no capacitors to charge and discharge during large-signal excursions, R_F and R_{IN} determine the VEA gain. Use the following equation to calculate the value for R_F:

$$R_F = \frac{I_{OUT} \times R_{IN}}{N \times G_C \times \Delta V_{OUT}} \quad (25)$$

$$G_C = \frac{0.05}{R_S} \quad (26)$$

where G_C is the current-loop transconductance and N is number of phases.

When designing the current-control loop ensure that the inductor downslope (when it becomes an upslope at the CEA output) does not exceed the ramp slope. This is a necessary condition to avoid sub-harmonic oscillations similar to those in peak current-mode control with insufficient slope compensation. Use the following equation to calculate the resistor R_{CF}:

$$R_{CF} \le \frac{2 \times f_{SW} \times L \times 10^2}{V_{OUT} \times R_{SENSE}} \quad (27)$$

For example, the maximum R_{CF} is 12kΩ for R_{SENSE} = 1.35mΩ.

C_{CF} provides a low-frequency pole while R_{CF} provides a midband zero. Place a zero at f_Z to obtain a phase bump at the crossover frequency. Place a high-frequency pole

(f_P) at least a decade away from the crossover frequency to achieve maximum phase margin.

Use the following equations to calculate C_{CF} and C_{CFF}:

$$C_{CF} = \frac{1}{2 \times \pi \times f_Z \times R_{CF}} \quad (28)$$

$$C_{CFF} = \frac{1}{2 \times \pi \times f_P \times R_{CF}} \quad (29)$$

PC Board Layout

Use the following guidelines to layout the switching voltage regulator:

1) Place the V_{IN} and V_{CC} bypass capacitors close to the MAX5065/MAX5067.
2) Minimize the area and length of the high-current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep short the current loop from the lower-switching MOSFET, inductor, and output capacitor.
4) Place the Schottky diodes close to the lower MOSFETs and on the same side of the PC board.
5) Keep the SGND and PGND isolated and connect them at one single point close to the negative terminal of the input-filter capacitor.
6) Run the current-sense lines CS+ and CS- very close to each other to minimize the loop area. Similarly, run the remote-voltage sense lines SENSE+ and SENSE- close to each other. Do not cross these critical signal lines through power circuitry. Sense the current right at the pads of the current-sense resistors.
7) Avoid long traces between the V_{CC} bypass capacitors, driver output of the MAX5065/MAX5067, MOSFET gates and PGND pin. Minimize the loop formed by the V_{CC} bypass capacitors, bootstrap diode, bootstrap capacitor, MAX5065/MAX5067, and upper MOSFET gate.
8) Place the bank of output capacitors close to the load.
9) Distribute the power components evenly across the board for proper heat dissipation.
10) Provide enough copper area at and around the switching MOSFETs, inductor, and sense resistors to aid in thermal dissipation.
11) Use at least 4oz copper to keep the trace inductance and resistance to a minimum. Thin copper PC boards can compromise efficiency since high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.

Chip Information

TRANSISTOR COUNT: 5451

PROCESS: BiCMOS

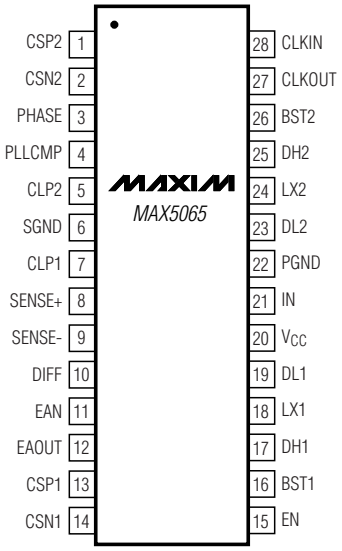
Selector Guide

PART	OUTPUT
MAX5065	Adjustable +0.6V to +3.3V
MAX5067	Adjustable +0.8V to +3.3V with OVP, PGOOD, Phase Failure Detector

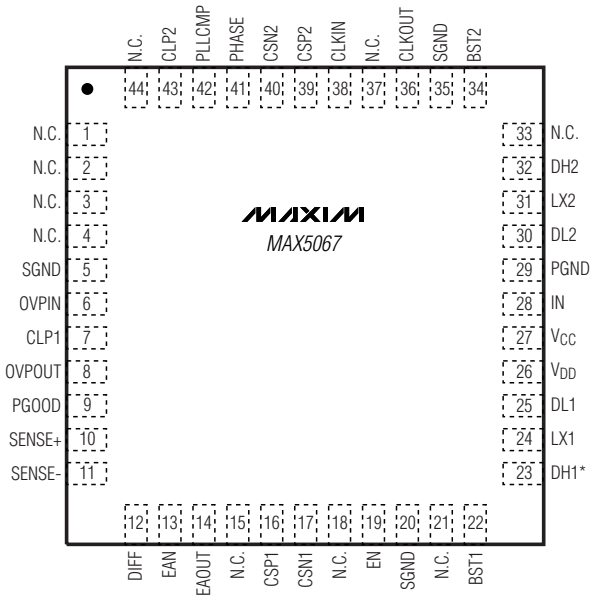
Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

Pin Configurations

TOP VIEW



28 SSOP



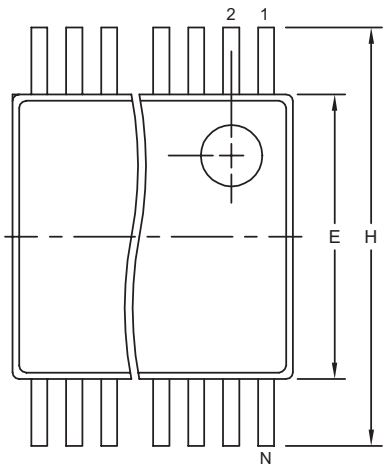
44 THIN QFN*

*CONNECT THE THIN QFN EXPOSED PAD TO SGND GROUND PLANE.

Package Information

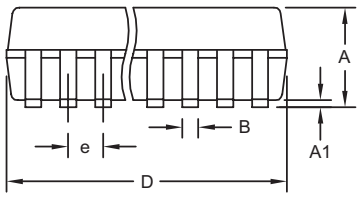
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.

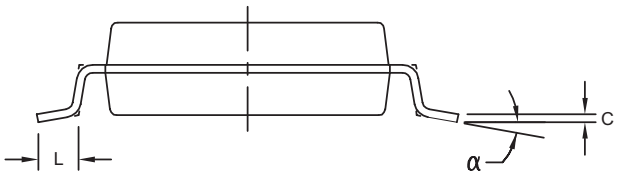
SSOP.EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

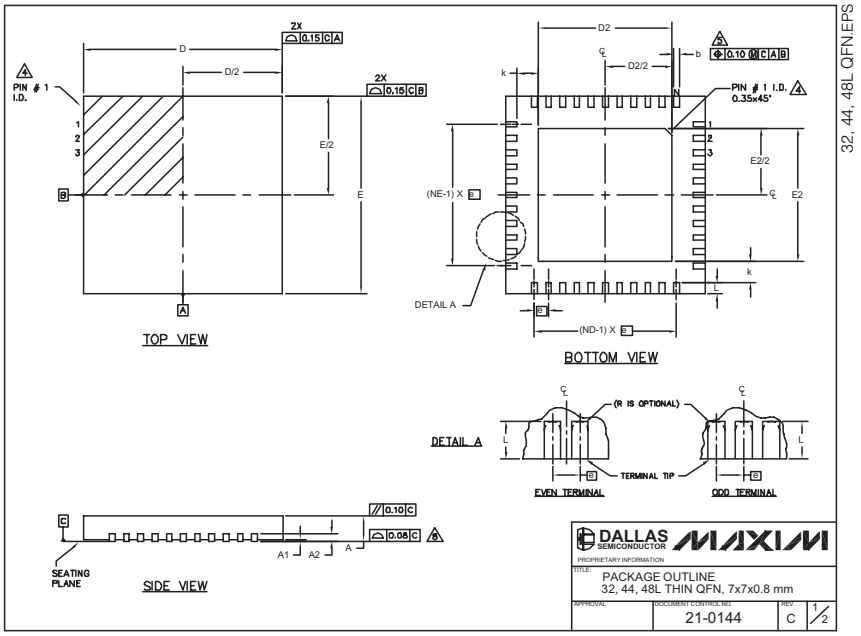
PACKAGE OUTLINE, SSOP, 5.3 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0056	C	1/1

Dual-Phase, +0.6V to +3.3V Output Parallelable, Average-Current-Mode Controllers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477-1; T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	–
T4877-2	–	5.46	5.60	5.63	5.46	5.60	5.63	–
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T3277-1, T4877-1; T4877-2 & T4877-3.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 32, 44, 48L THIN QFN, 7x7x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0144 | REV. C | 2/2